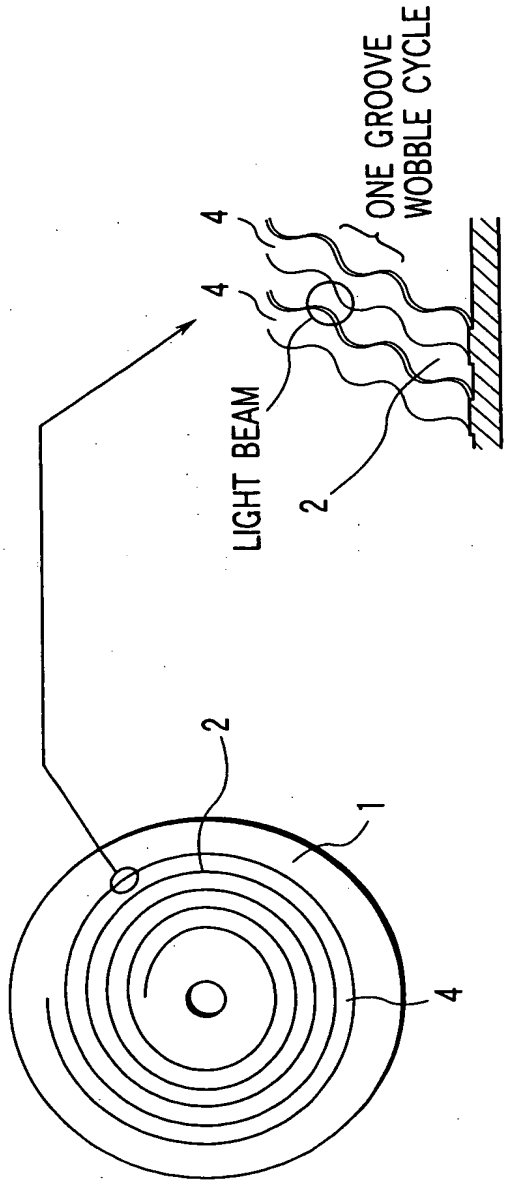


FIG. 1

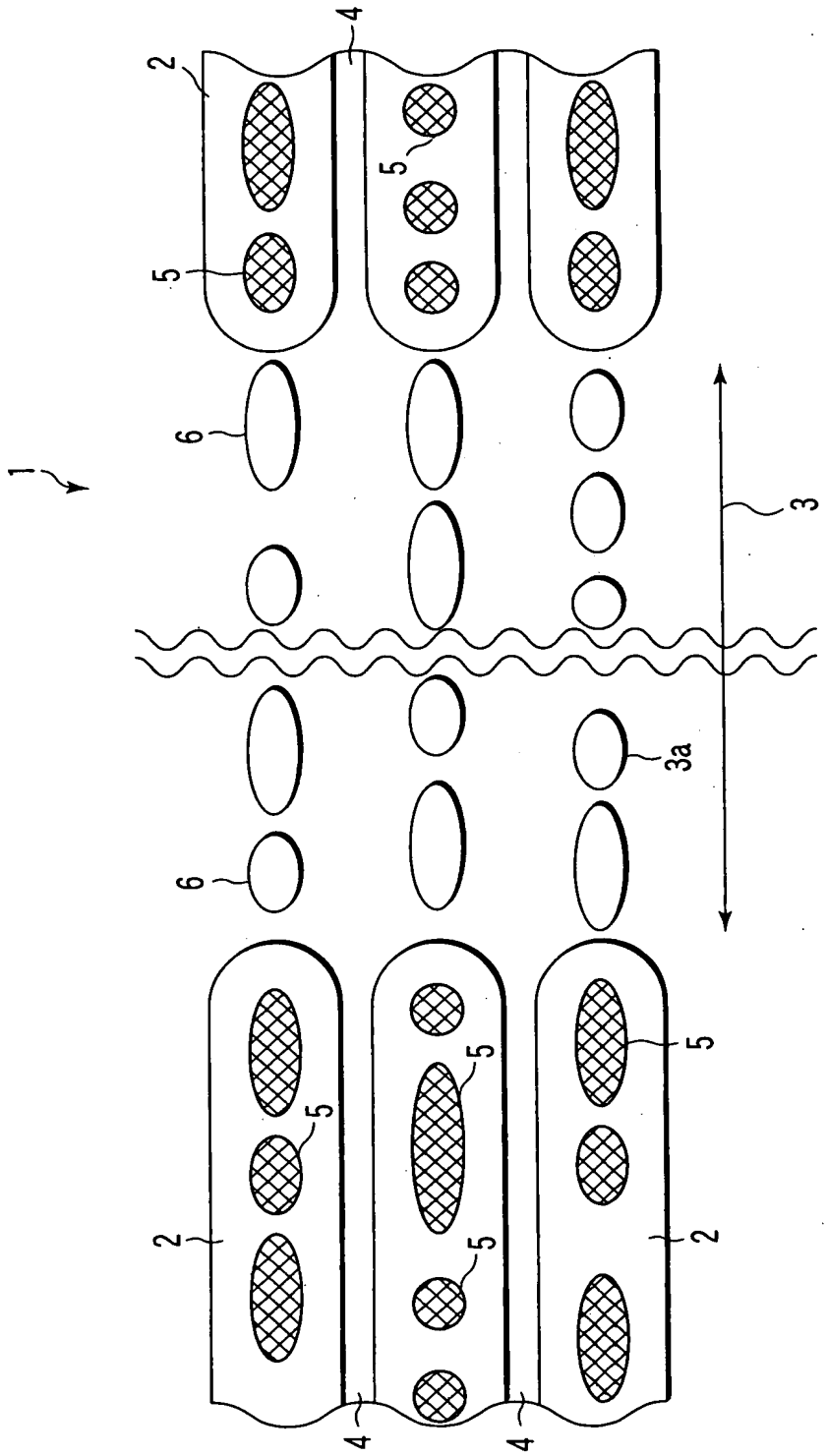


FIG. 2

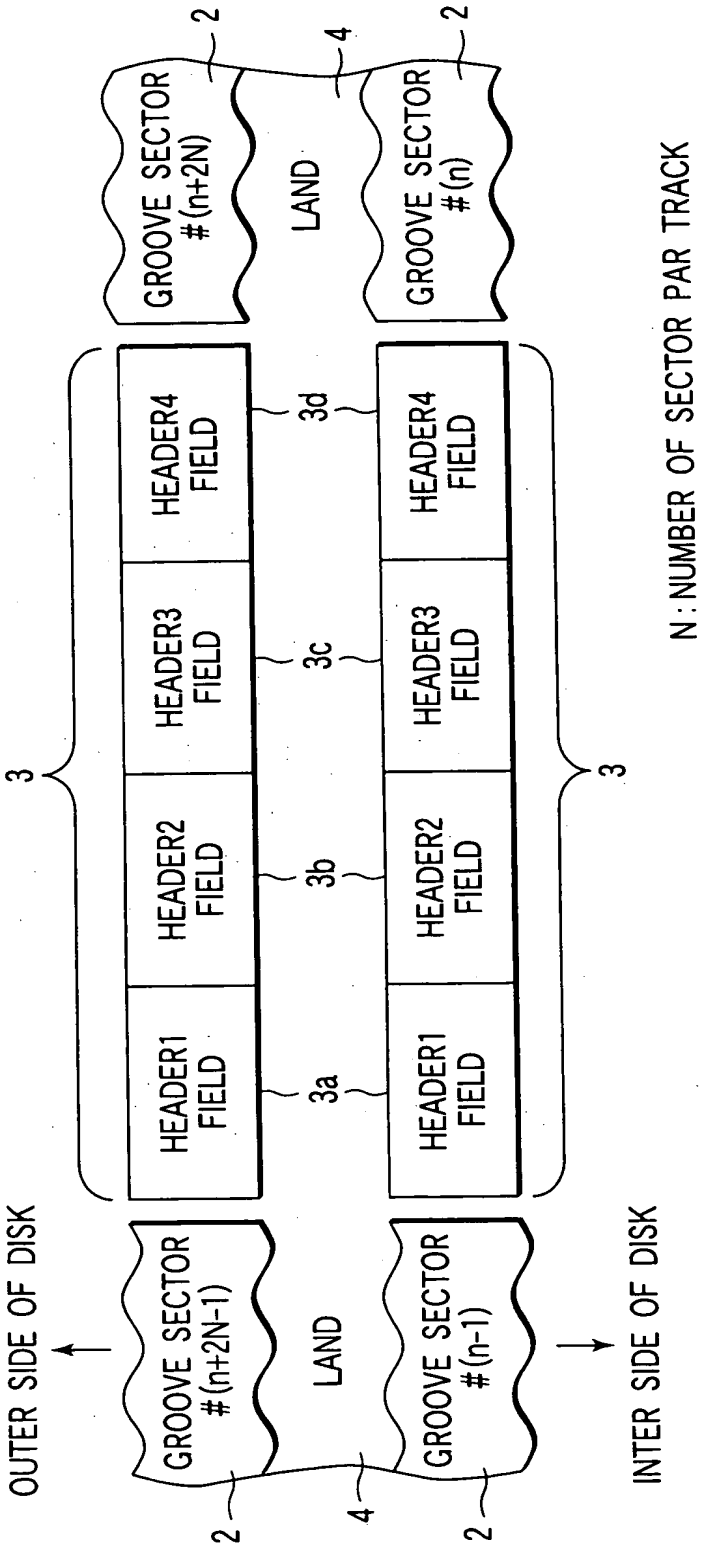

OUTER SIDE OF DISK
INTER SIDE OF DISK
GROOVE SECTOR #(n+2N-1)
LAND
GROOVE SECTOR #(n-1)
GROOVE SECTOR #(n+2N)
LAND
GROOVE SECTOR #(n)
HEADER1 FIELD
HEADER2 FIELD
HEADER3 FIELD
HEADER4 FIELD
3
3a
3b
3c
3d
2
4
N : NUMBER OF SECTOR PAR TRACK

FIG. 3

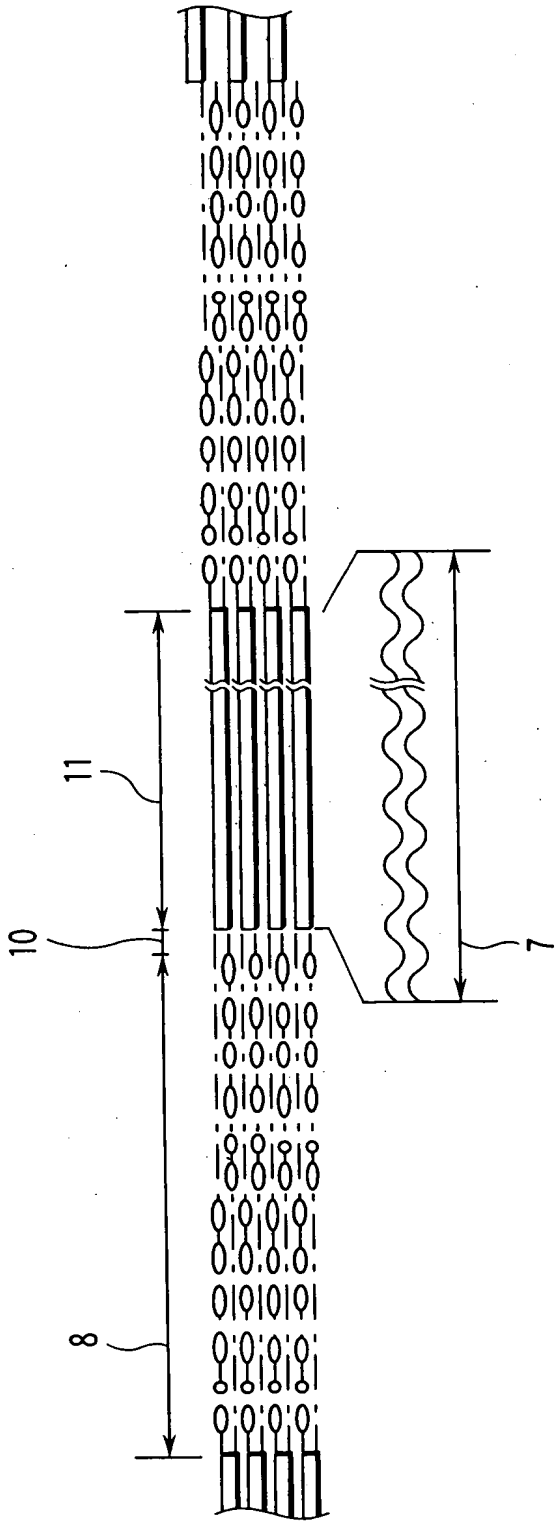


FIG. 4

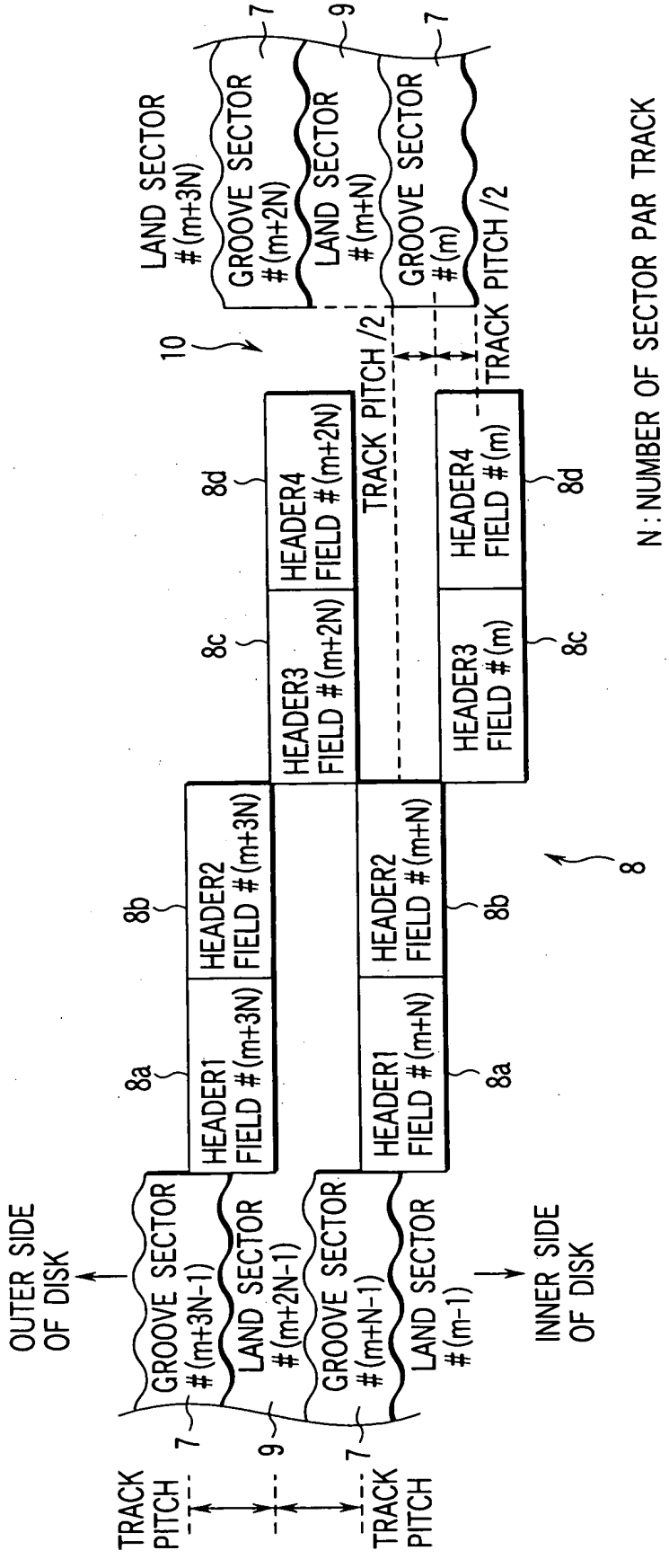

OUTER SIDE OF DISK
INNER SIDE OF DISK
TRACK PITCH
TRACK PITCH
GROOVE SECTOR #(m+3N-1)
LAND SECTOR #(m+2N-1)
GROOVE SECTOR #(m+N-1)
LAND SECTOR #(m-1)
HEADER1 FIELD #(m+3N)
HEADER2 FIELD #(m+3N)
HEADER1 FIELD #(m+N)
HEADER2 FIELD #(m+N)
HEADER3 FIELD #(m+2N)
HEADER4 FIELD #(m+2N)
HEADER3 FIELD #(m)
HEADER4 FIELD #(m)
TRACK PITCH /2
TRACK PITCH /2
LAND SECTOR #(m+3N)
GROOVE SECTOR #(m+2N)
LAND SECTOR #(m+N)
GROOVE SECTOR #(m)
TRACK PITCH
7
9
7
8a
8b
8c
8d
8
10
N : NUMBER OF SECTOR PAR TRACK

FIG. 5

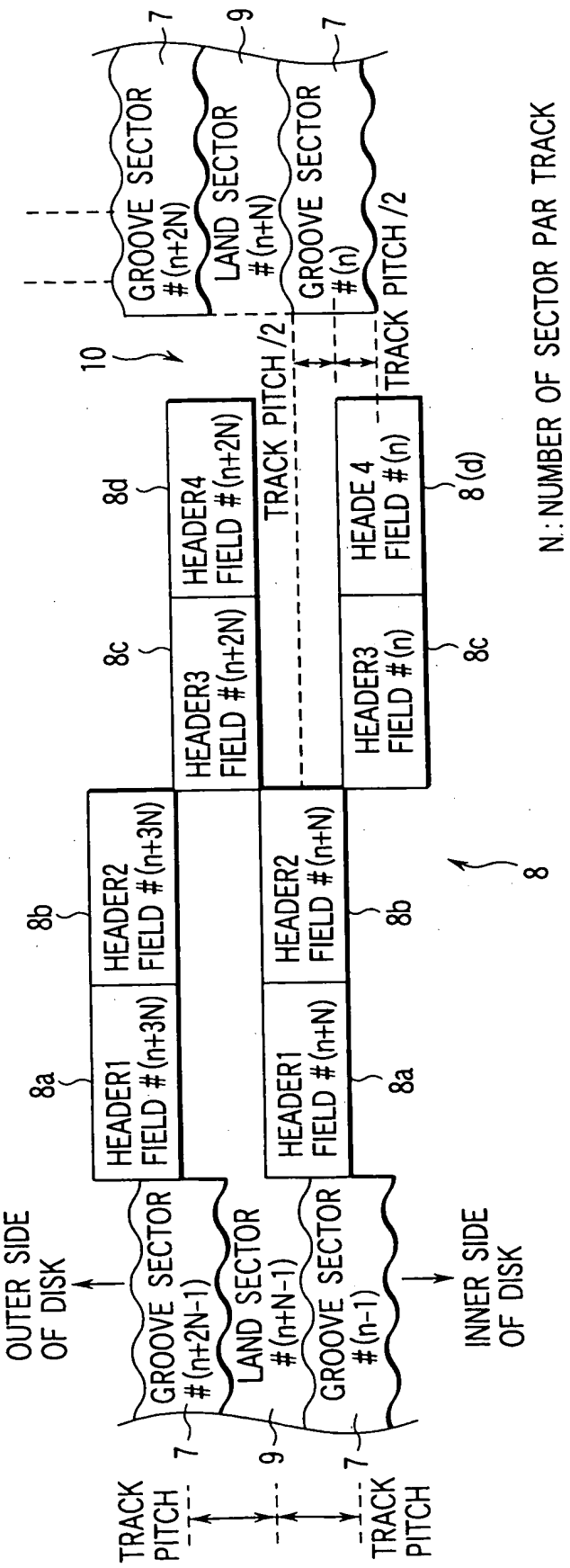

OUTER SIDE OF DISK
INNER SIDE OF DISK
GROOVE SECTOR #(n+2N-1)
LAND SECTOR #(n+N-1)
GROOVE SECTOR #(n-1)
GROOVE SECTOR #(n+2N)
LAND SECTOR #(n+N)
GROOVE SECTOR #(n)
TRACK PITCH
TRACK PITCH /2
HEADER1 FIELD #(n+3N)
HEADER2 FIELD #(n+3N)
HEADER3 FIELD #(n+2N)
HEADER4 FIELD #(n+2N)
HEADER1 FIELD #(n+N)
HEADER2 FIELD #(n+N)
HEADER3 FIELD #(n)
HEADE 4 FIELD #(n)
8
8a
8b
8c
8d
8(d)
7
9
10
N: NUMBER OF SECTOR PAR TRACK

FIG. 6

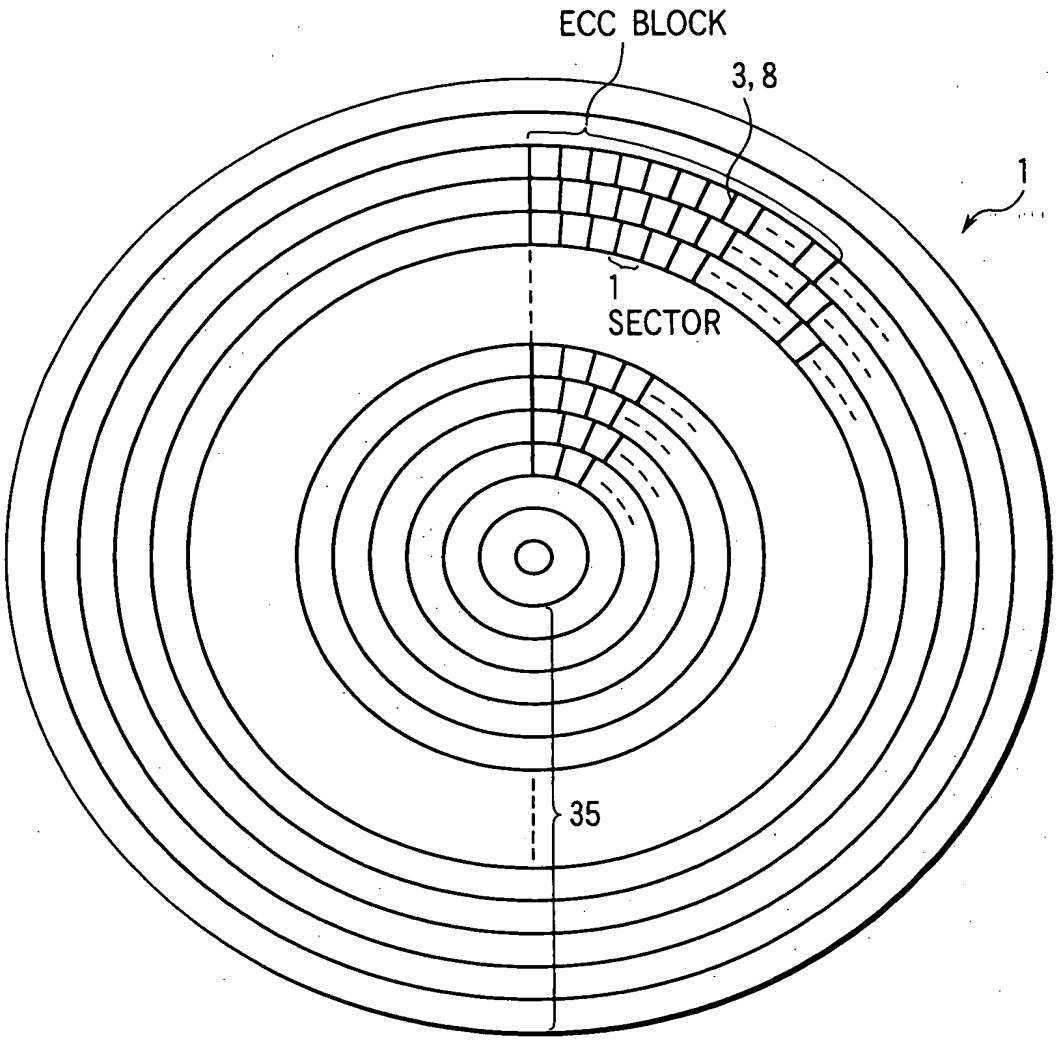


FIG. 7

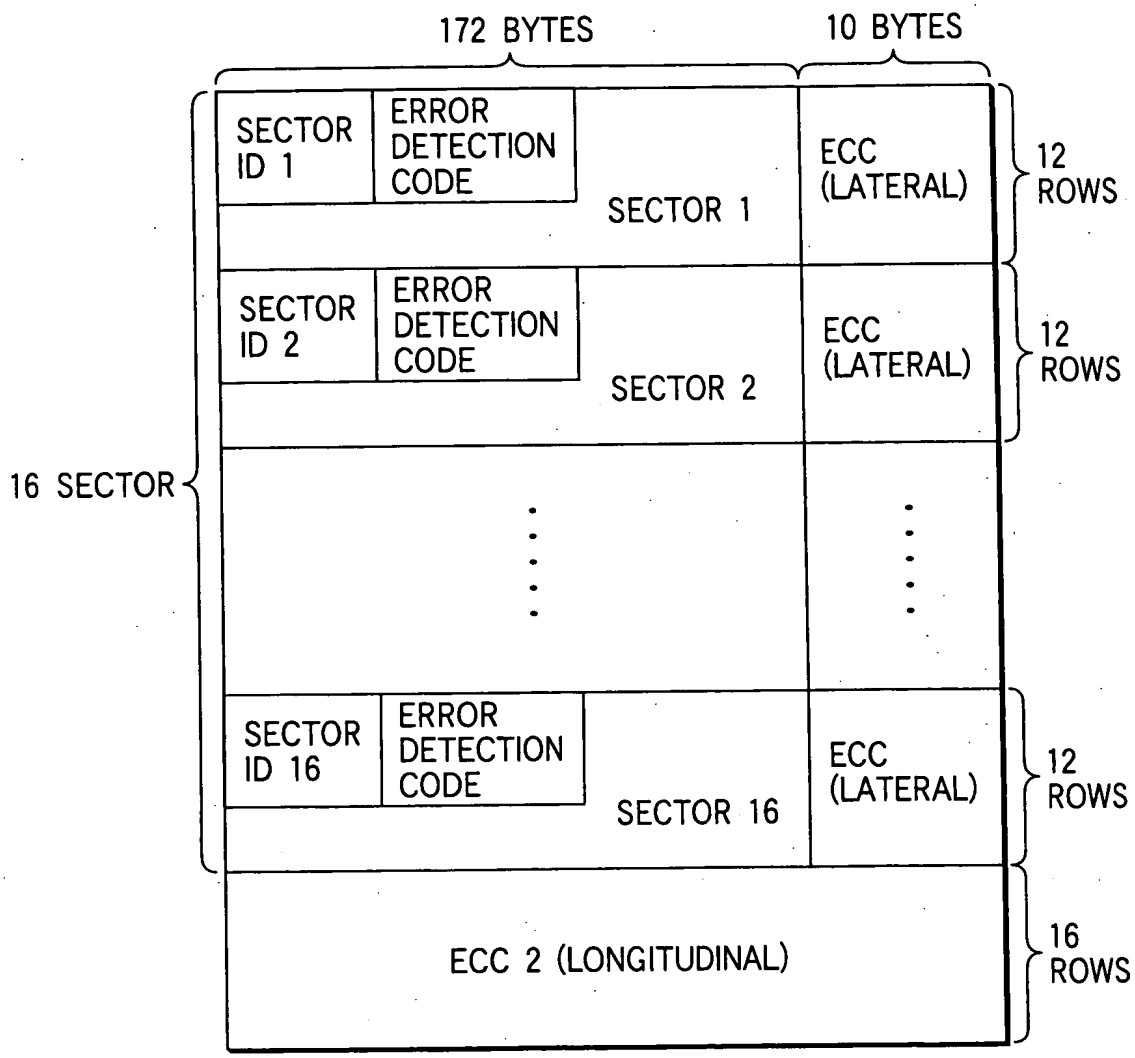

172 BYTES
10 BYTES
16 SECTOR
SECTOR ID 1
ERROR DETECTION CODE
SECTOR 1
ECC (LATERAL)
12 ROWS
SECTOR ID 2
ERROR DETECTION CODE
SECTOR 2
ECC (LATERAL)
12 ROWS
SECTOR ID 16
ERROR DETECTION CODE
SECTOR 16
ECC (LATERAL)
12 ROWS
ECC 2 (LONGITUDINAL)
16 ROWS

FIG. 8

	SYNC FRAME		SYNC FRAME	
	32 CHANNEL BITS (2 BYTES)	1456 CHANNEL BITS (91 BYTES)	32 CHANNEL BITS (2 BYTES)	1456 CHANNEL BITS (91 BYTES)
13 ROWS	SY0	ZERO FRAME	SY5	FIRST FRAME
	SY1		SY5	
	SY2		SY5	
	SY3		SY5	
	SY4		SY5	
	SY1		SY6	
	SY2		SY6	
	SY3		SY6	
	SY4		SY6	
	SY1		SY7	
	SY2		SY7	
	SY3		SY7	
	SY4		SY7	

FIG. 9

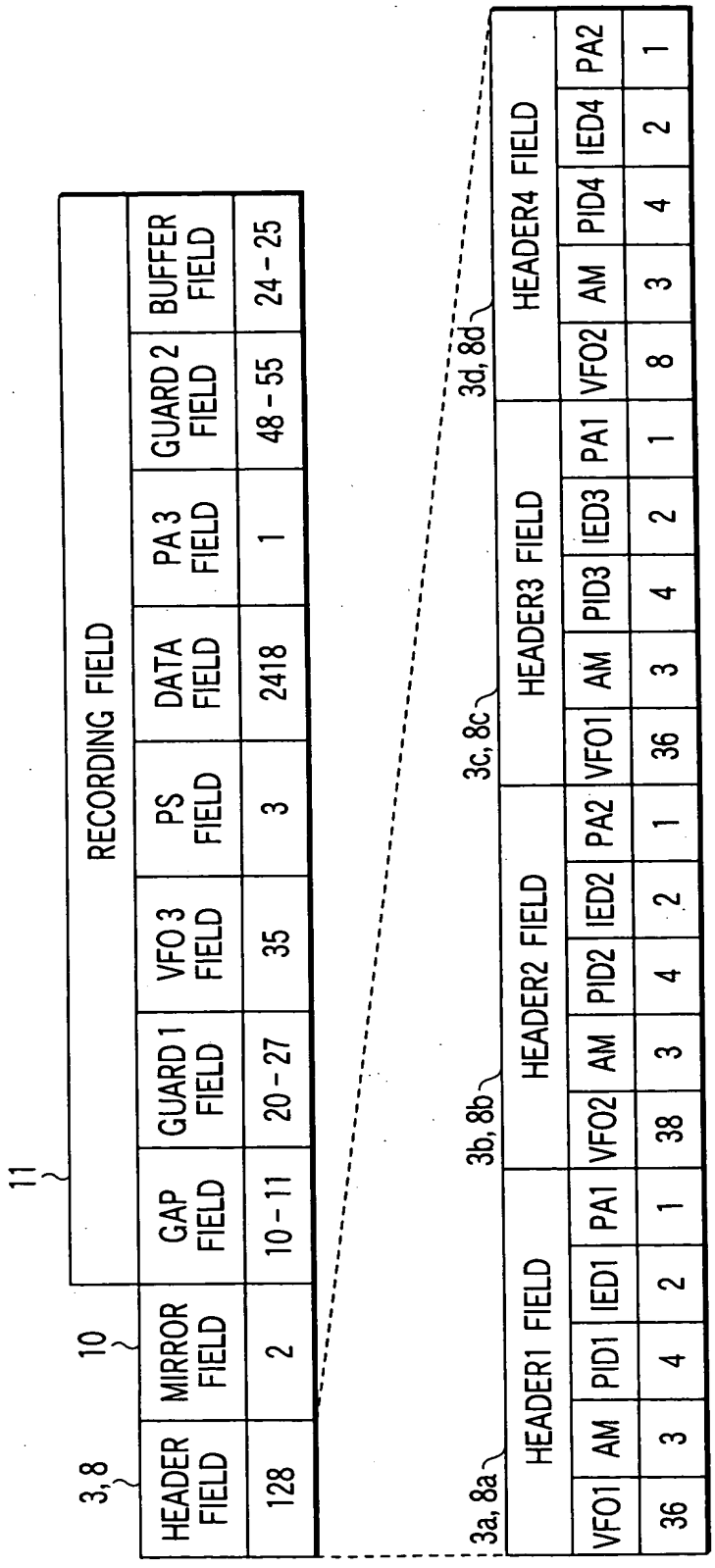

11
RECORDING FIELD
3, 8
HEADER FIELD
10
MIRROR FIELD
GAP FIELD
GUARD 1 FIELD
VFO 3 FIELD
PS FIELD
DATA FIELD
PA 3 FIELD
GUARD 2 FIELD
BUFFER FIELD
128
2
10 - 11
20 - 27
35
3
2418
1
48 - 55
24 - 25
3a, 8a
HEADER1 FIELD
VFO1
AM
PID1
IED1
PA1
36
3
4
2
1
3b, 8b
HEADER2 FIELD
VFO2
AM
PID2
IED2
PA2
38
3
4
2
1
3c, 8c
HEADER3 FIELD
VFO1
AM
PID3
IED3
PA1
36
3
4
2
1
3d, 8d
HEADER4 FIELD
VFO2
AM
PID4
IED4
PA2
8
3
4
2
1

FIG. 10

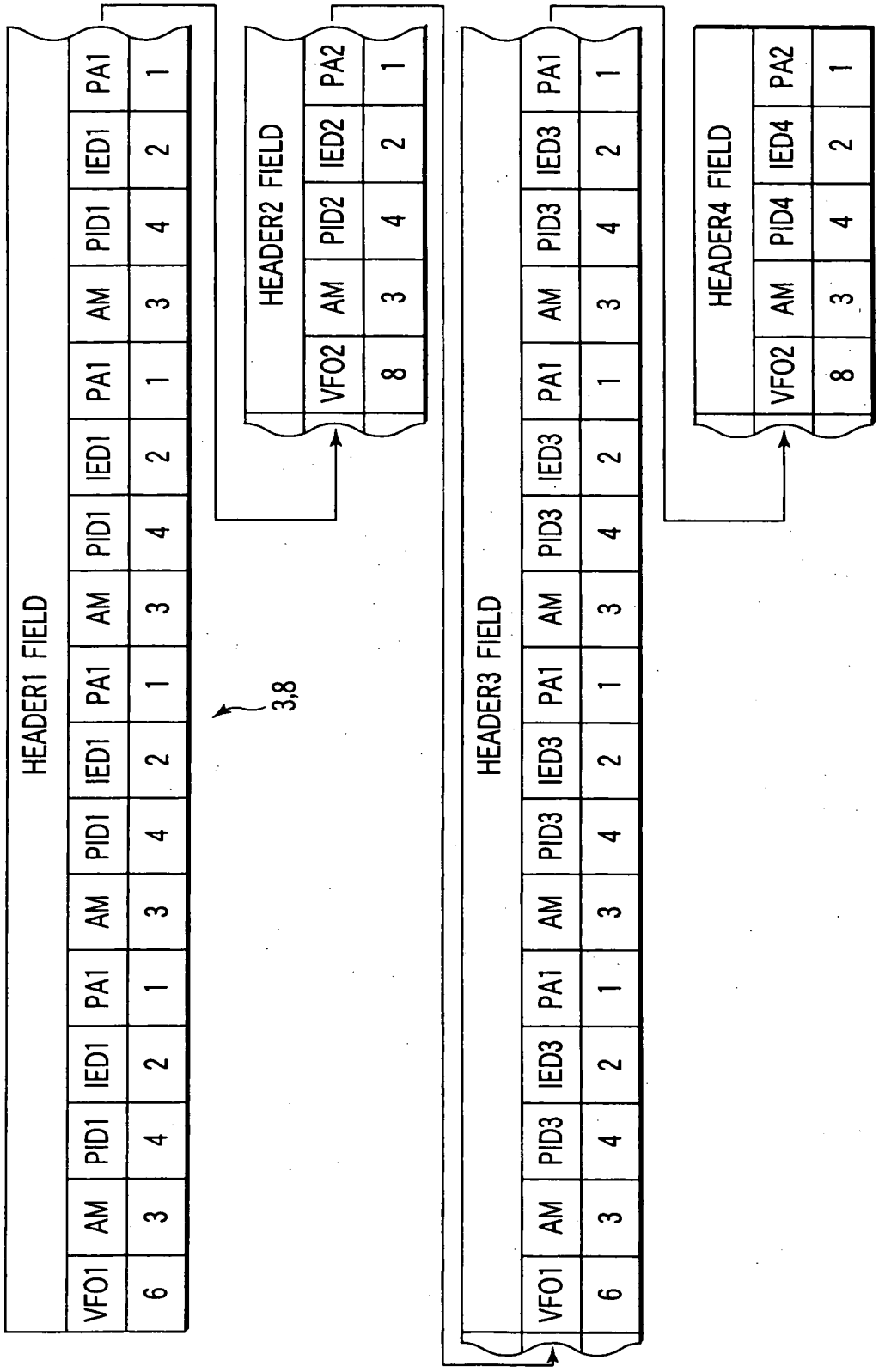

HEADER1 FIELD
VFO1 AM PID1 IED1 PA1 AM PID1 IED1 PA1 AM PID1 IED1 PA1
6 3 4 2 1 3 4 2 1 3 4 2 1
HEADER2 FIELD
VFO2 AM PID2 IED2 PA2
8 3 4 2 1
HEADER3 FIELD
VFO1 AM PID3 IED3 PA1 AM PID3 IED3 PA1 AM PID3 IED3 PA1
6 3 4 2 1 3 4 2 1 3 4 2 1
HEADER4 FIELD
VFO2 AM PID4 IED4 PA2
8 3 4 2 1
3,8

FIG. 11

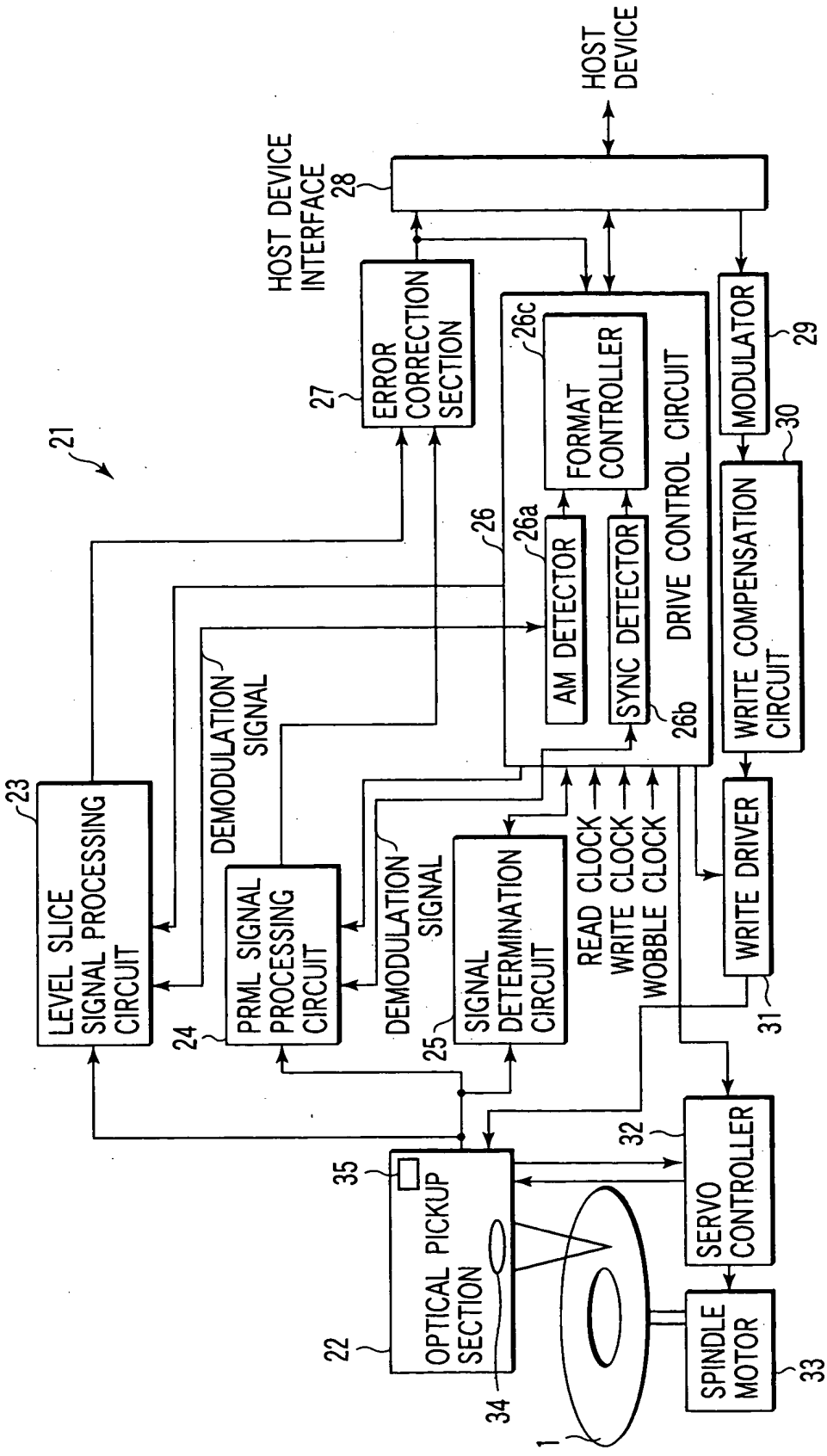

HOST DEVICE
HOST DEVICE INTERFACE
28
ERROR CORRECTION SECTION
27
21
DRIVE CONTROL CIRCUIT
26
26a
AM DETECTOR
26c
FORMAT CONTROLLER
SYNC DETECTOR
26b
MODULATOR
29
30
WRITE COMPENSATION CIRCUIT
WRITE DRIVER
31
23
LEVEL SLICE SIGNAL PROCESSING CIRCUIT
DEMODULATION SIGNAL
24
PRML SIGNAL PROCESSING CIRCUIT
DEMODULATION SIGNAL
25
SIGNAL DETERMINATION CIRCUIT
READ CLOCK
WRITE CLOCK
WOBBLE CLOCK
32
SERVO CONTROLLER
35
OPTICAL PICKUP SECTION
22
34
1
SPINDLE MOTOR
33

FIG. 12

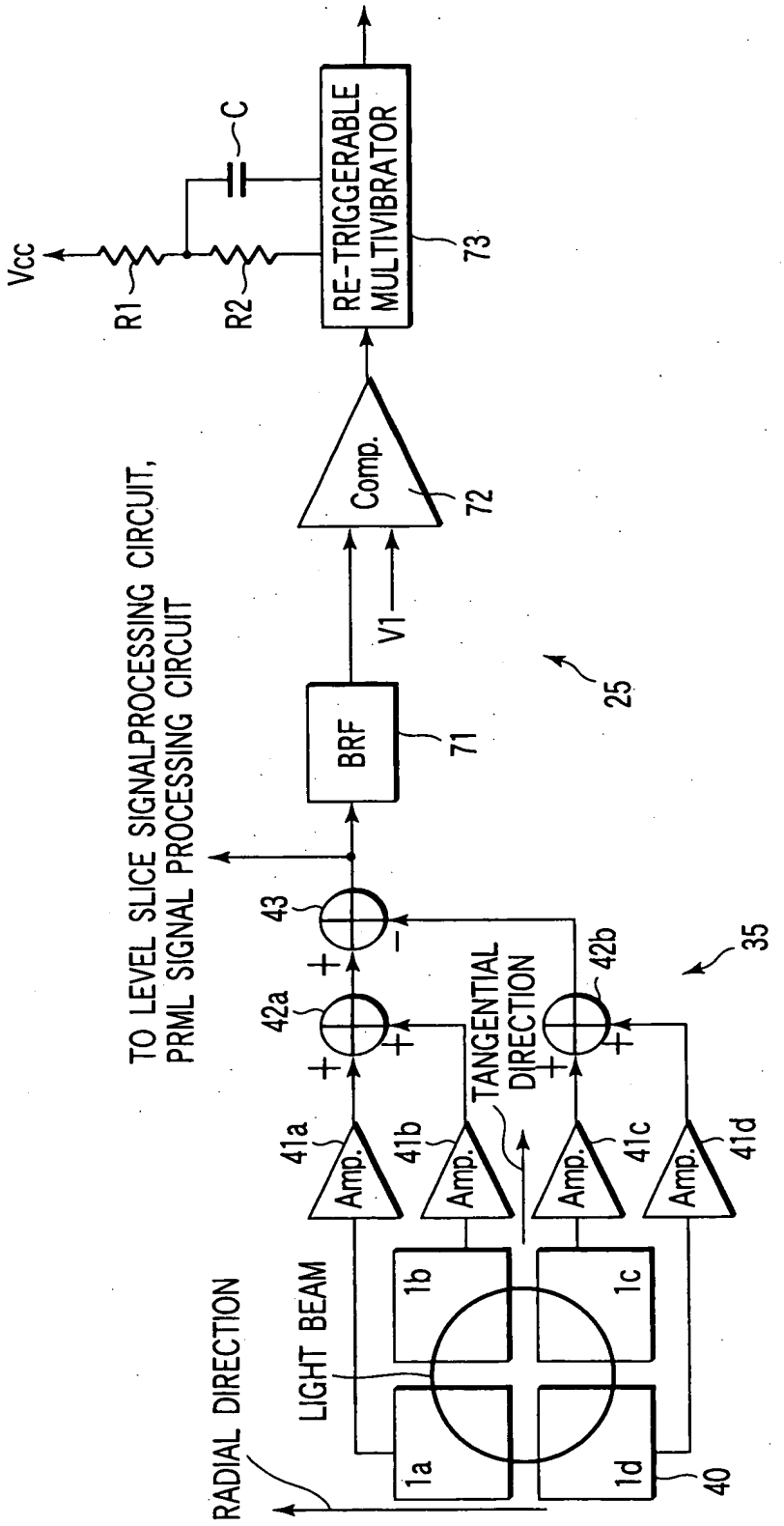

Vcc
R1
R2
C
RE-TRIGGERABLE MULTIVIBRATOR
73
Comp.
72
V1
BRF
71
25
TO LEVEL SLICE SIGNALPROCESSING CIRCUIT, PRML SIGNAL PROCESSING CIRCUIT
43
42a
42b
35
TANGENTIAL DIRECTION
41a
41b
41c
41d
Amp.
LIGHT BEAM
1a
1b
1c
1d
40
RADIAL DIRECTION

FIG. 13

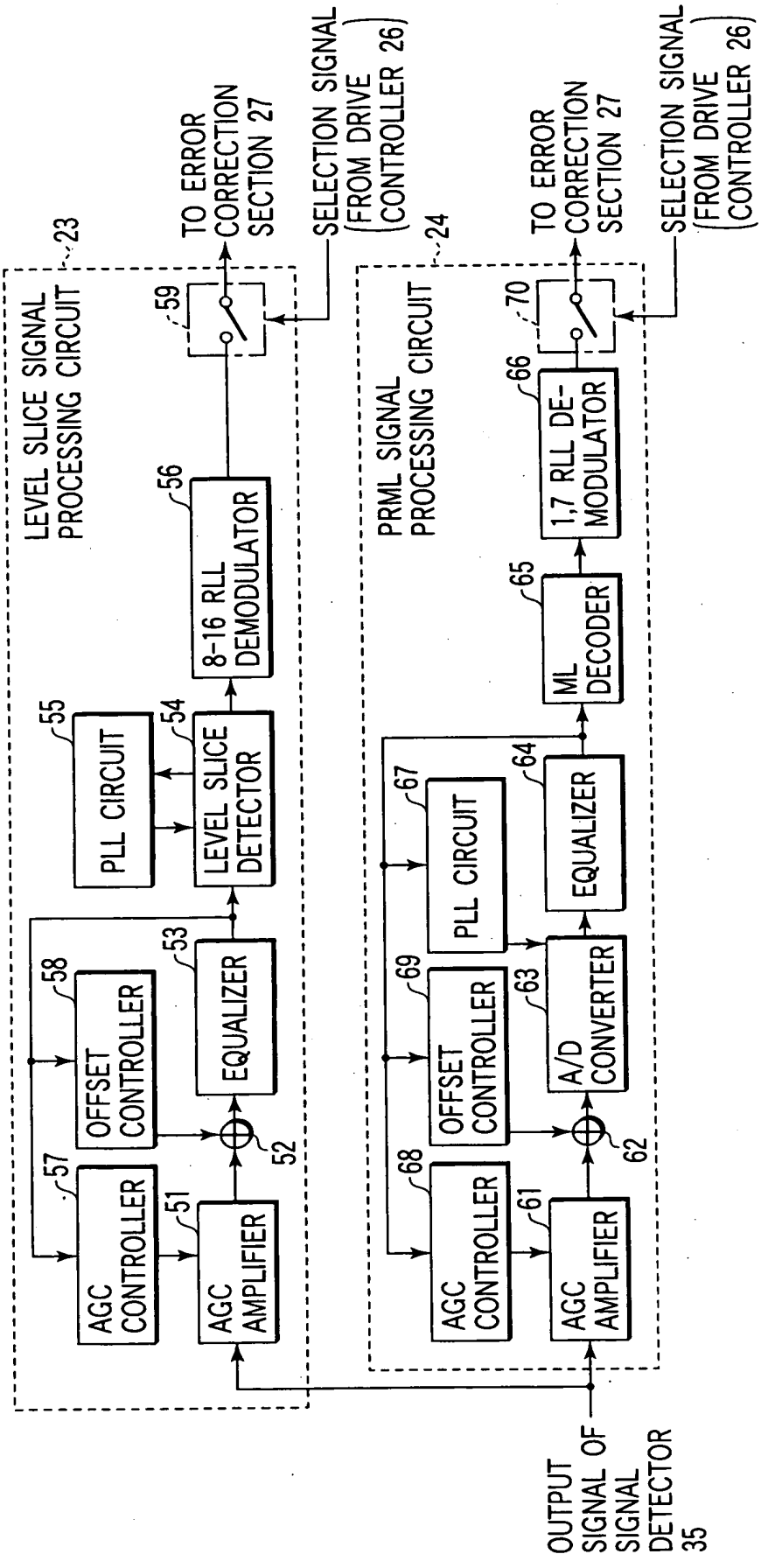

LEVEL SLICE SIGNAL PROCESSING CIRCUIT
23
AGC CONTROLLER
57
AGC AMPLIFIER
51
OFFSET CONTROLLER
58
EQUALIZER
53
52
PLL CIRCUIT
55
LEVEL SLICE DETECTOR
54
8-16 RLL DEMODULATOR
56
59
TO ERROR CORRECTION SECTION 27
SELECTION SIGNAL (FROM DRIVE CONTROLLER 26)
PRML SIGNAL PROCESSING CIRCUIT
24
AGC CONTROLLER
68
AGC AMPLIFIER
61
OFFSET CONTROLLER
69
A/D CONVERTER
63
62
PLL CIRCUIT
67
EQUALIZER
64
ML DECODER
65
1,7 RLL DE-MODULATOR
66
70
TO ERROR CORRECTION SECTION 27
SELECTION SIGNAL (FROM DRIVE CONTROLLER 26)
OUTPUT SIGNAL OF SIGNAL DETECTOR 35

FIG. 14

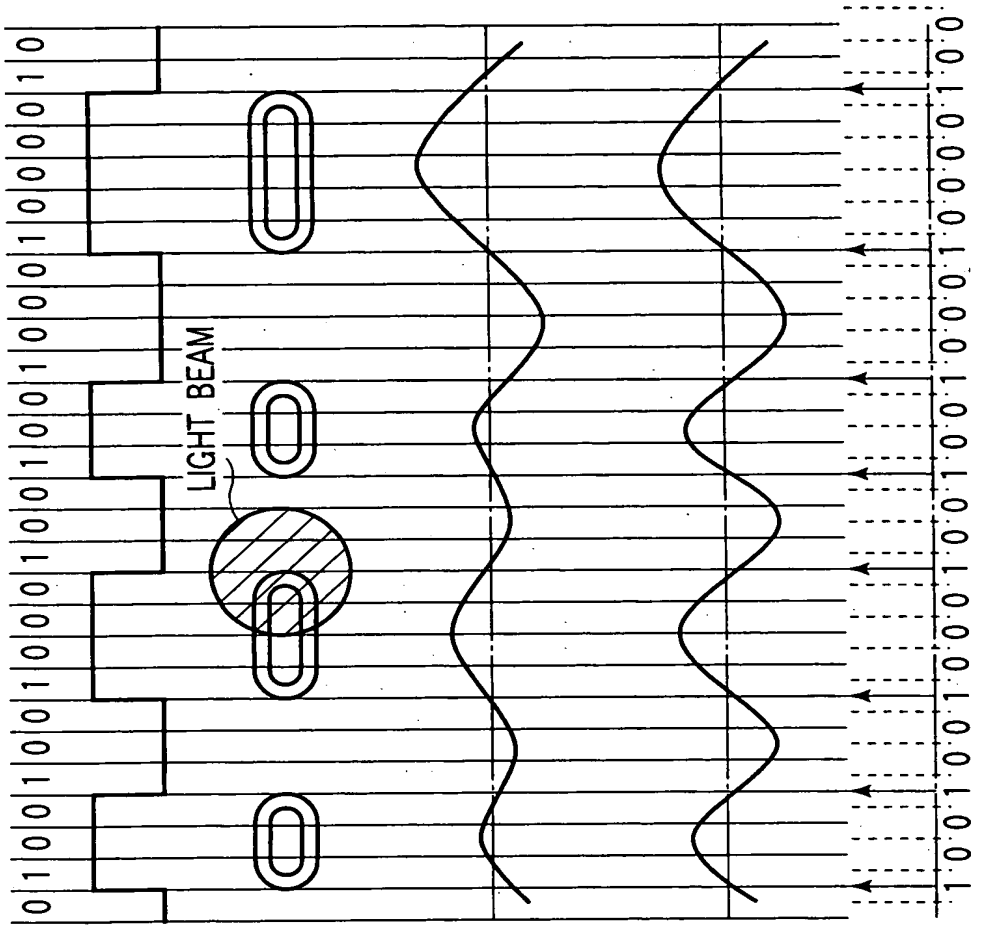


FIG. 15A RECORDING DATA

FIG. 15B RECORDING WAVEFORM

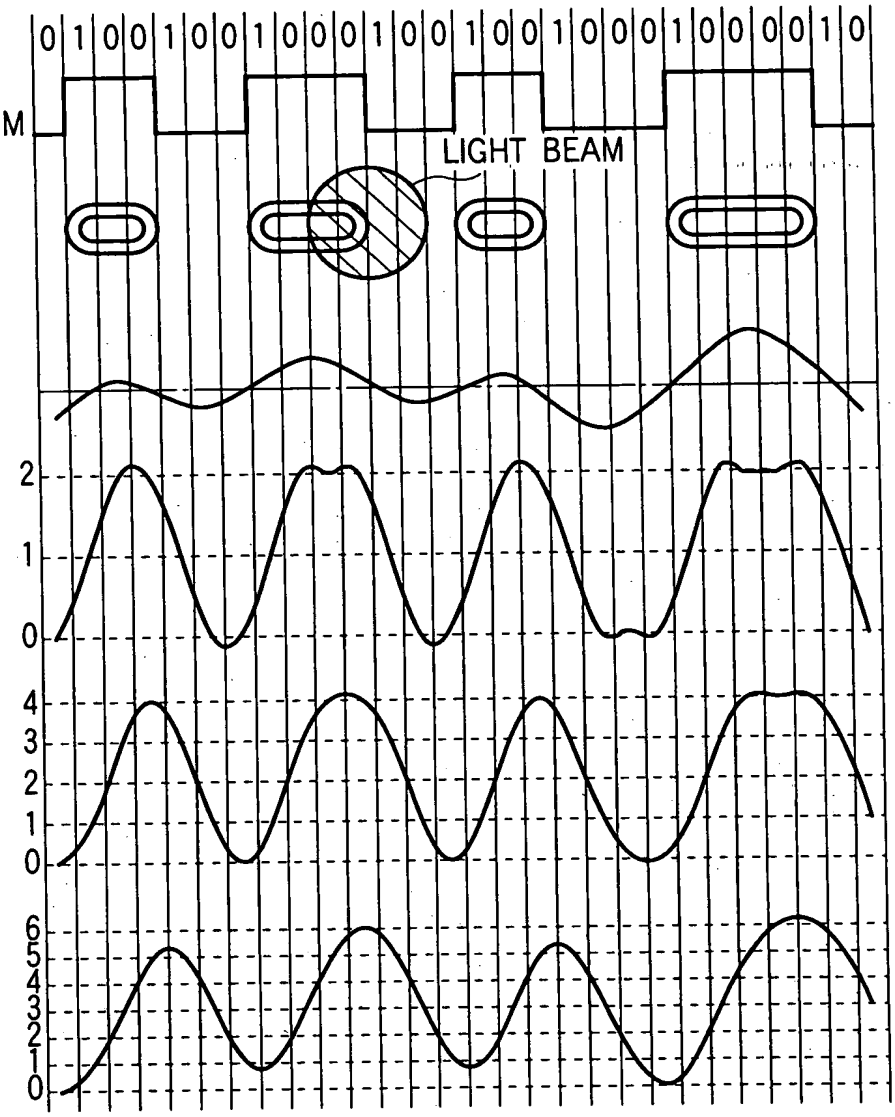
FIG. 15C PIT SERIES

FIG. 15D REPRODUCED WAVEFORM

FIG. 15E EQUALIZED WAVEFORM

FIG. 15F BINARY DATA FOR DETECTION OF INTERSECTION

RECORDING DATA
FIG. 16A
RECORDING WAVEFORM
FIG. 16B
PIT SERIES
FIG. 16C
REPRODUCED WAVEFORM
FIG. 16D
PR(1,1) CHARACTERISTIC
FIG. 16E
PR(1,2,1) CHARACTERISTIC
FIG. 16F
PR(1,2,2,1) CHARACTERISTIC
FIG. 16G



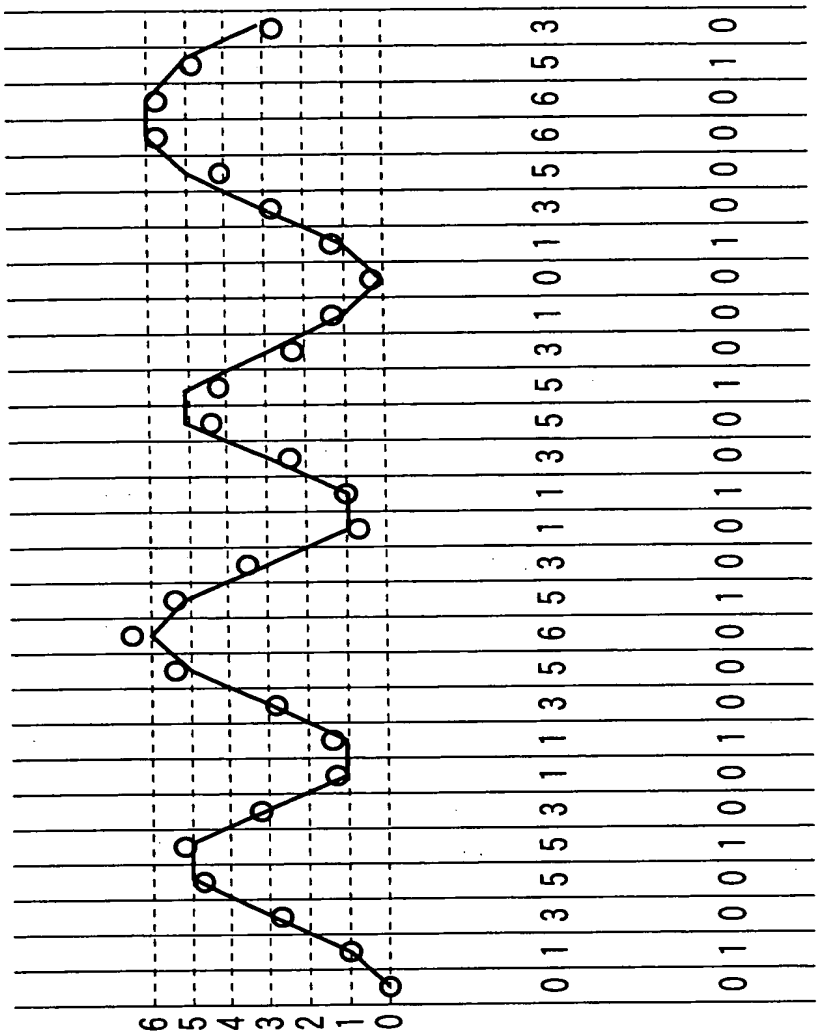


FIG. 17A EQUALIZED SIGNAL SAMPLE SERIES AND SERIES SELECTED BY VITERBI DECODER

FIG. 17B SIGNAL LEVEL OF SELECTED SERIES

FIG. 17C DECODED DATA

FIG. 18A OUTPUT SIGNAL OF PF

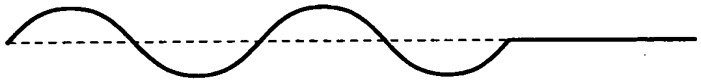


FIG. 18B

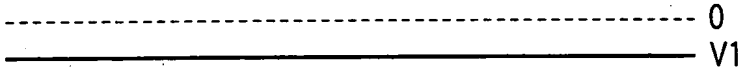


FIG. 18C OUTPUT SIGNAL OF COMPARATOR

FIG. 18D OUTPUT SIGNAL OF RE-TRIGGERABLE FF CIRCUIT

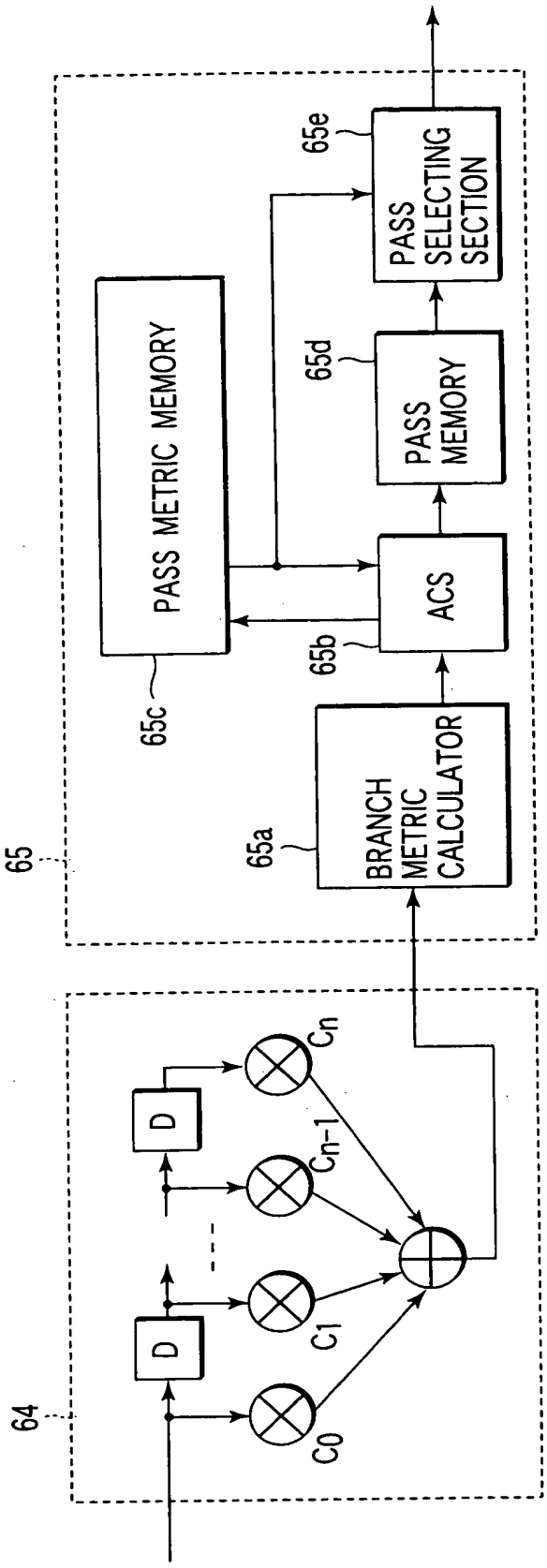

64
65
65a
BRANCH METRIC CALCULATOR
65b
ACS
65c
PASS METRIC MEMORY
65d
PASS MEMORY
65e
PASS SELECTING SECTION
D
D
C0
C1
Cn-1
Cn

FIG. 19

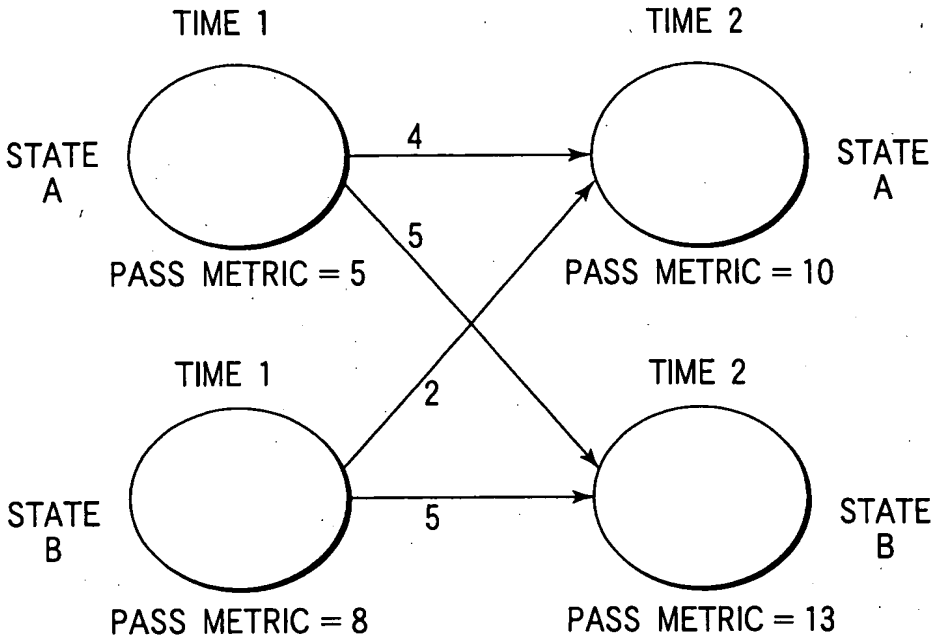

TIME 1
TIME 2
STATE A
STATE A
4
5
PASS METRIC = 5
PASS METRIC = 10
TIME 1
TIME 2
2
STATE B
STATE B
5
PASS METRIC = 8
PASS METRIC = 13

FIG. 20

FIG. 21A

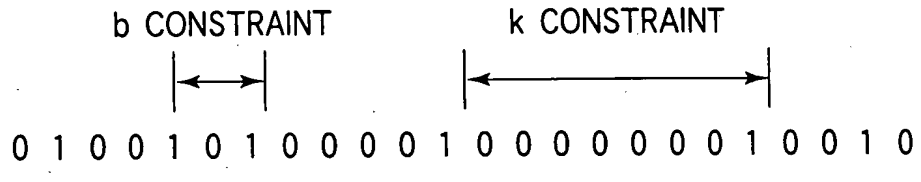
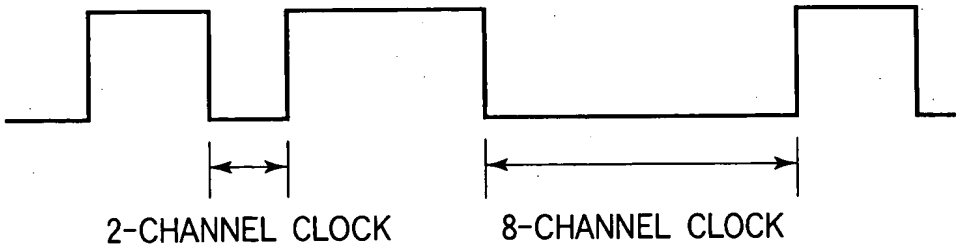


FIG. 21B



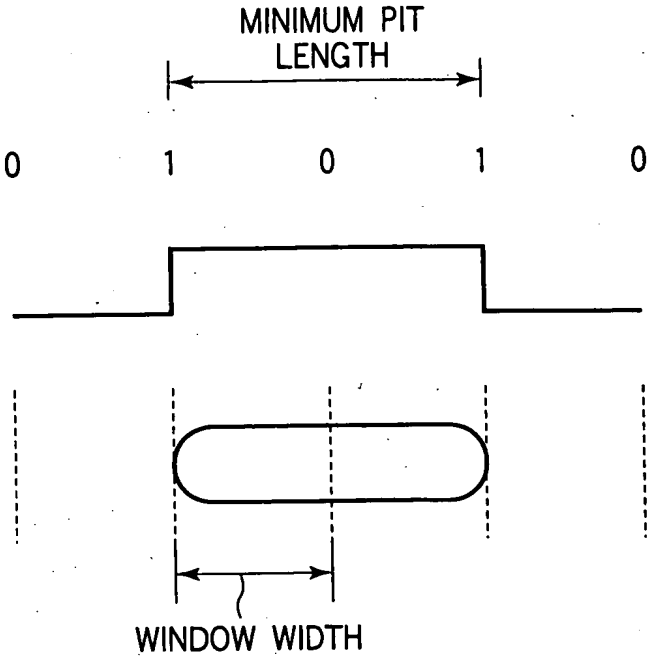


FIG. 22A

FIG. 22B

FIG. 22C

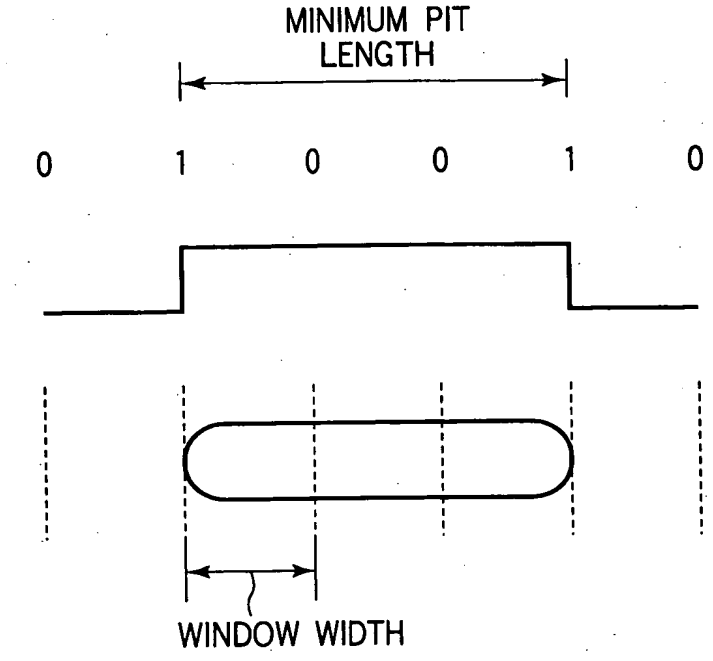


FIG. 22D

FIG. 22E

FIG. 22F

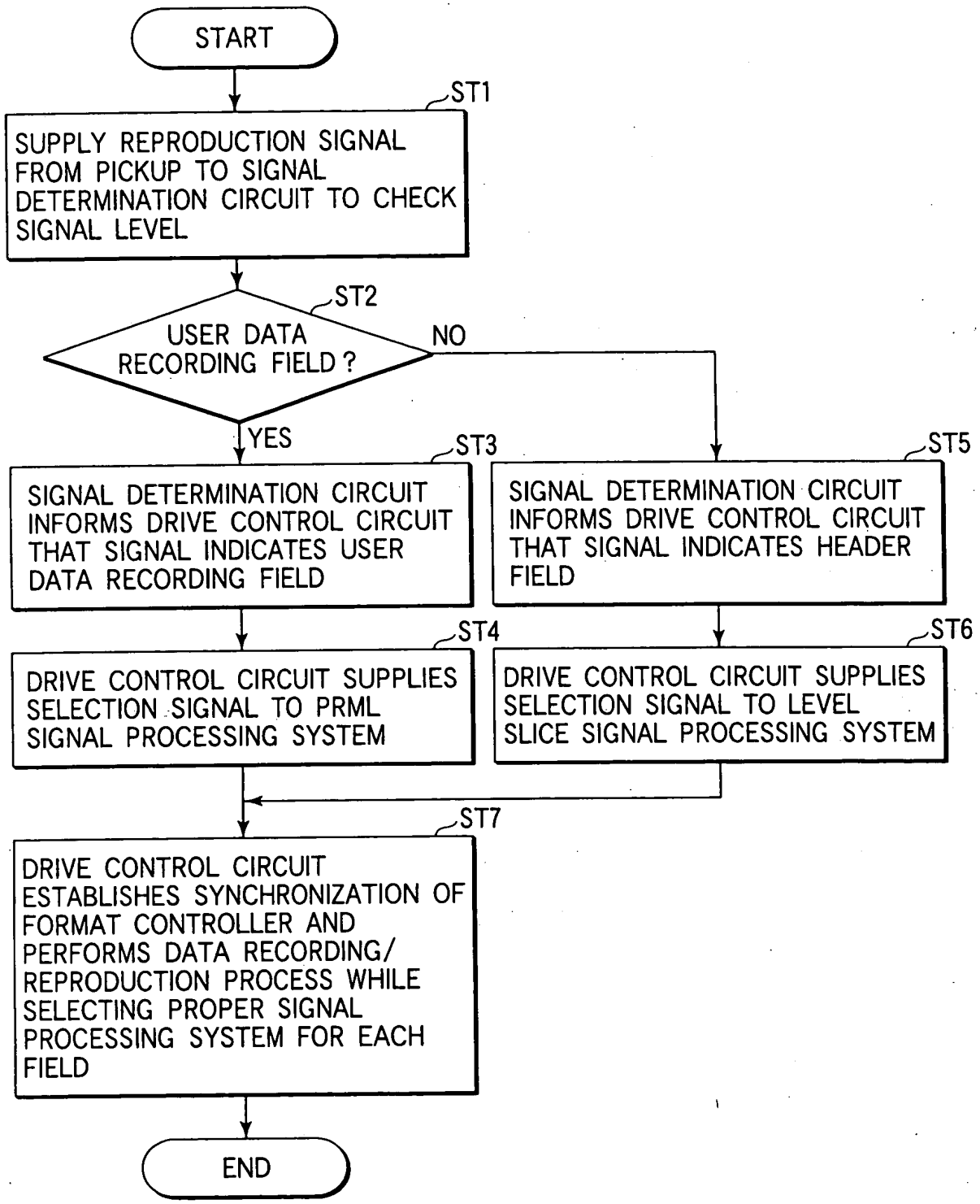

START
ST1
SUPPLY REPRODUCTION SIGNAL FROM PICKUP TO SIGNAL DETERMINATION CIRCUIT TO CHECK SIGNAL LEVEL
ST2
USER DATA RECORDING FIELD ?
NO
YES
ST3
SIGNAL DETERMINATION CIRCUIT INFORMS DRIVE CONTROL CIRCUIT THAT SIGNAL INDICATES USER DATA RECORDING FIELD
ST5
SIGNAL DETERMINATION CIRCUIT INFORMS DRIVE CONTROL CIRCUIT THAT SIGNAL INDICATES HEADER FIELD
ST4
DRIVE CONTROL CIRCUIT SUPPLIES SELECTION SIGNAL TO PRML SIGNAL PROCESSING SYSTEM
ST6
DRIVE CONTROL CIRCUIT SUPPLIES SELECTION SIGNAL TO LEVEL SLICE SIGNAL PROCESSING SYSTEM
ST7
DRIVE CONTROL CIRCUIT ESTABLISHES SYNCHRONIZATION OF FORMAT CONTROLLER AND PERFORMS DATA RECORDING/ REPRODUCTION PROCESS WHILE SELECTING PROPER SIGNAL PROCESSING SYSTEM FOR EACH FIELD
END

FIG. 23

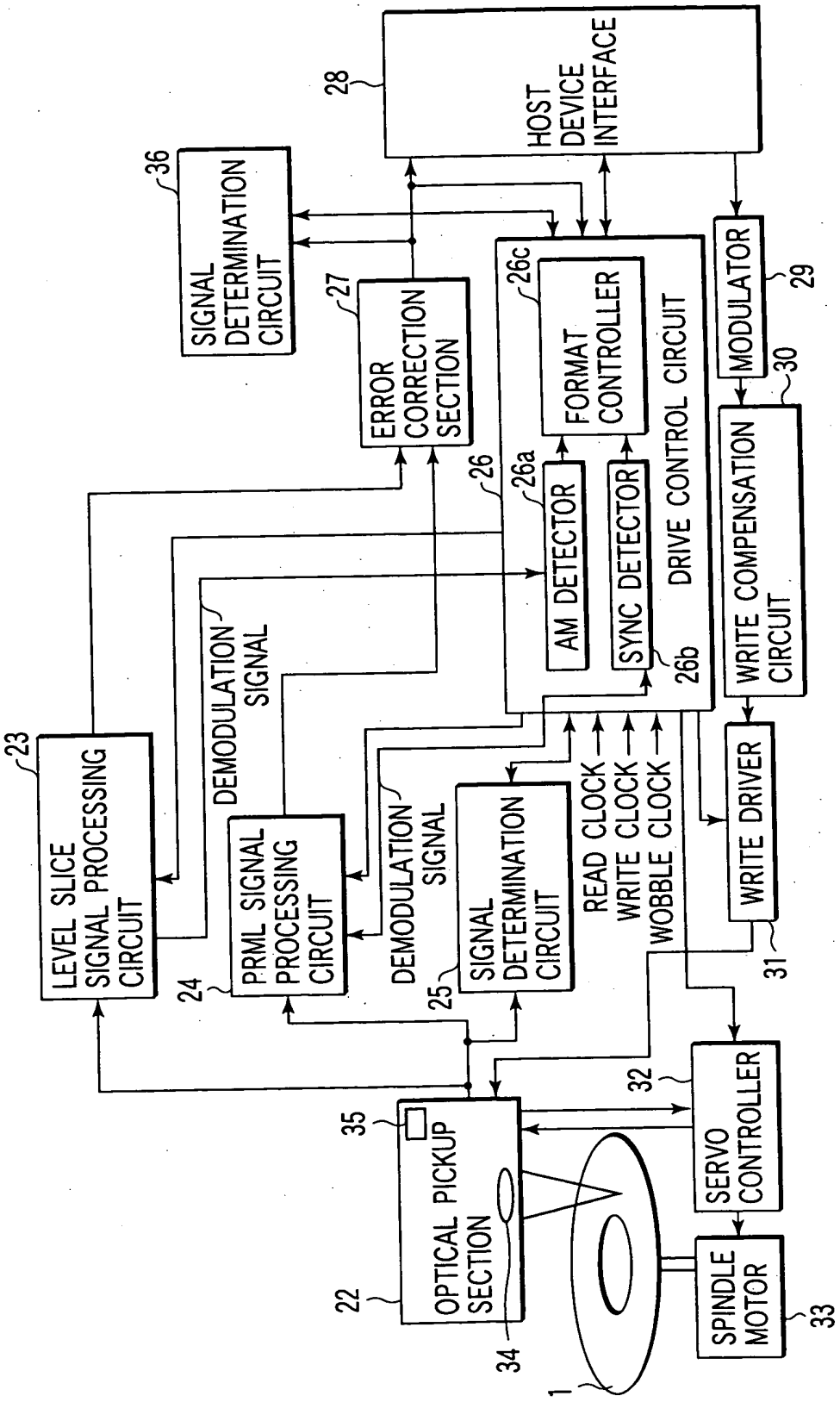

HOST DEVICE INTERFACE
28
SIGNAL DETERMINATION CIRCUIT
36
ERROR CORRECTION SECTION
27
DRIVE CONTROL CIRCUIT
26
26c
FORMAT CONTROLLER
26a
AM DETECTOR
SYNC DETECTOR
26b
MODULATOR
29
30
WRITE COMPENSATION CIRCUIT
WRITE DRIVER
31
LEVEL SLICE SIGNAL PROCESSING CIRCUIT
23
PRML SIGNAL PROCESSING CIRCUIT
24
SIGNAL DETERMINATION CIRCUIT
25
DEMODULATION SIGNAL
DEMODULATION SIGNAL
READ CLOCK
WRITE CLOCK
WOBBLE CLOCK
SERVO CONTROLLER
32
OPTICAL PICKUP SECTION
22
35
34
SPINDLE MOTOR
33
1

FIG. 24

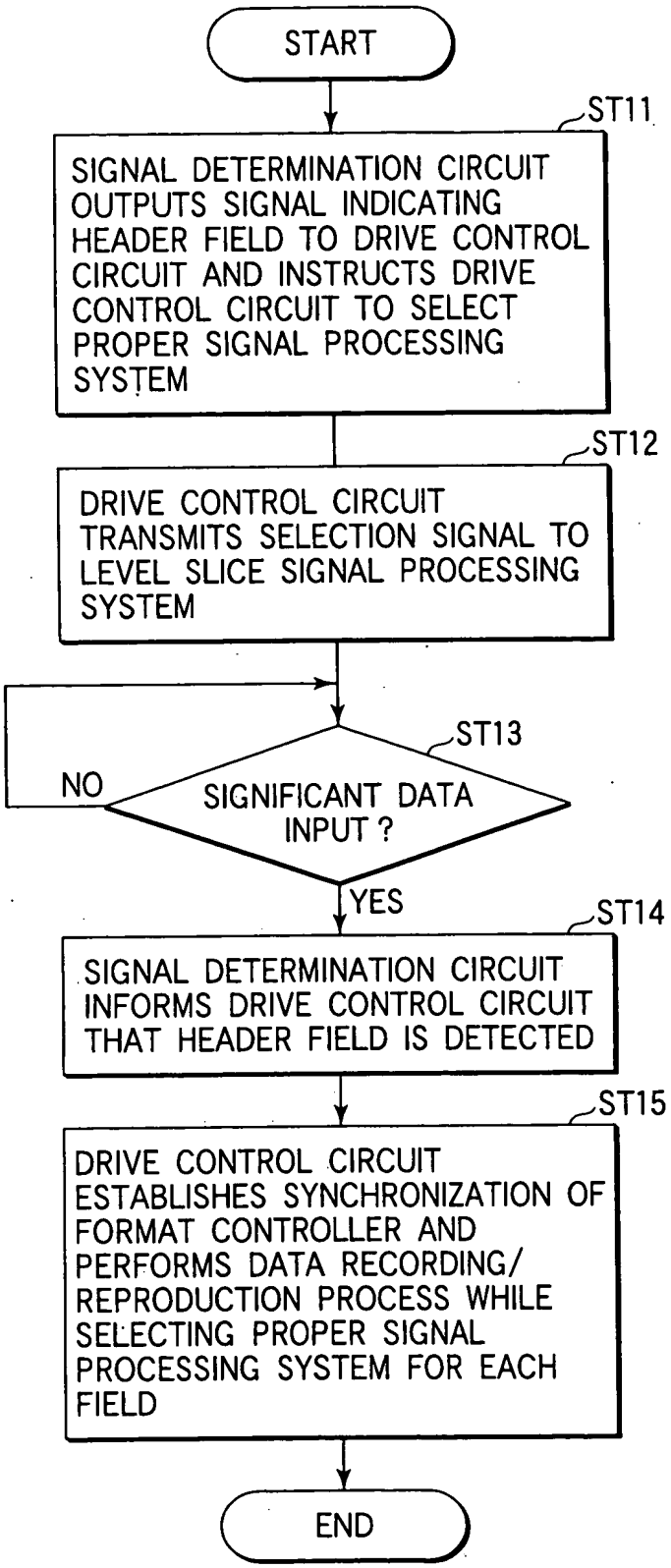

START
ST11
SIGNAL DETERMINATION CIRCUIT OUTPUTS SIGNAL INDICATING HEADER FIELD TO DRIVE CONTROL CIRCUIT AND INSTRUCTS DRIVE CONTROL CIRCUIT TO SELECT PROPER SIGNAL PROCESSING SYSTEM
ST12
DRIVE CONTROL CIRCUIT TRANSMITS SELECTION SIGNAL TO LEVEL SLICE SIGNAL PROCESSING SYSTEM
ST13
NO
SIGNIFICANT DATA INPUT ?
YES
ST14
SIGNAL DETERMINATION CIRCUIT INFORMS DRIVE CONTROL CIRCUIT THAT HEADER FIELD IS DETECTED
ST15
DRIVE CONTROL CIRCUIT ESTABLISHES SYNCHRONIZATION OF FORMAT CONTROLLER AND PERFORMS DATA RECORDING/ REPRODUCTION PROCESS WHILE SELECTING PROPER SIGNAL PROCESSING SYSTEM FOR EACH FIELD
END

FIG. 25

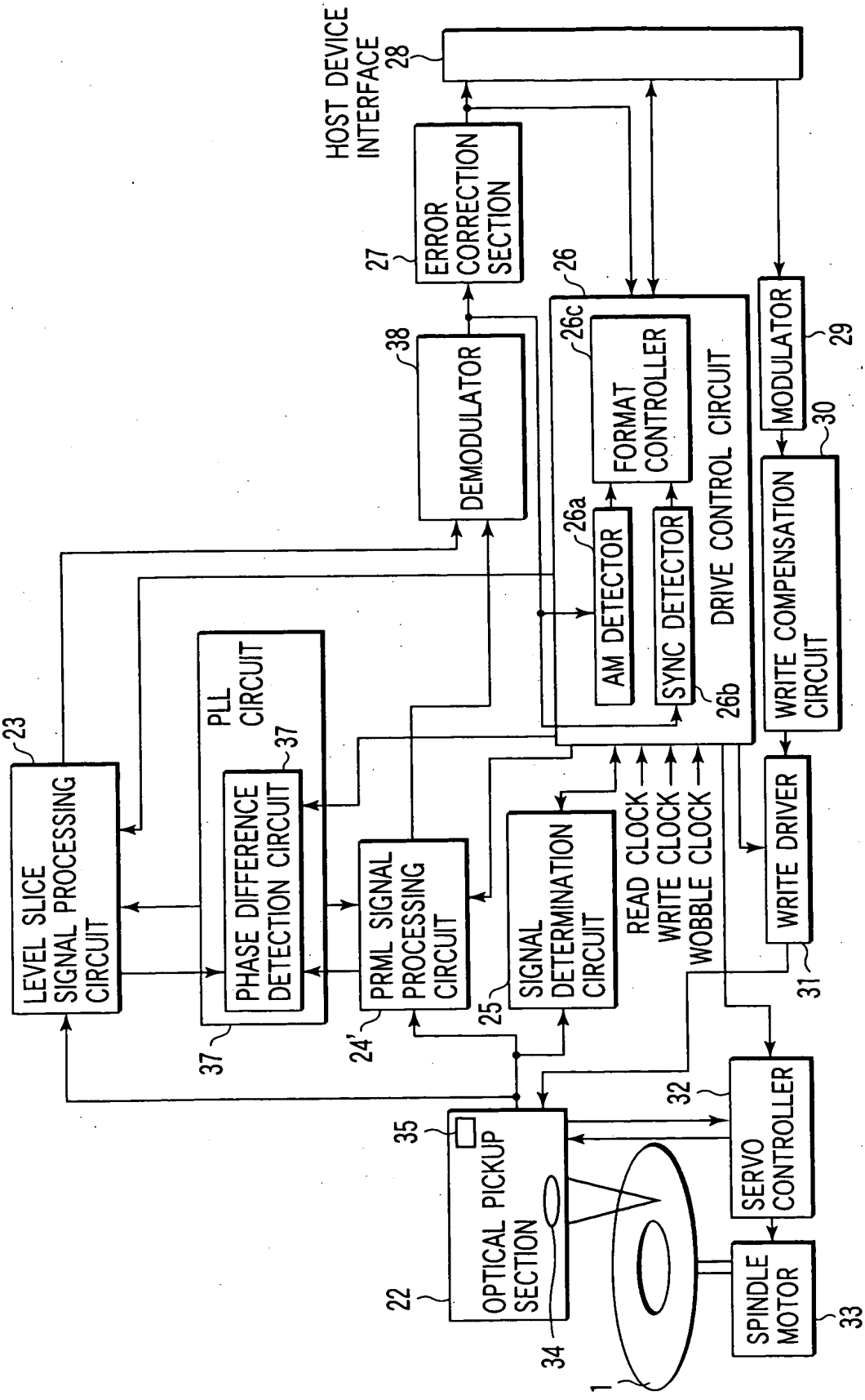

HOST DEVICE INTERFACE
28
ERROR CORRECTION SECTION
27
26
DEMODULATOR
38
26c
FORMAT CONTROLLER
MODULATOR
29
30
26a
AM DETECTOR
SYNC DETECTOR
26b
DRIVE CONTROL CIRCUIT
WRITE COMPENSATION CIRCUIT
23
LEVEL SLICE SIGNAL PROCESSING CIRCUIT
PLL CIRCUIT
37
PHASE DIFFERENCE DETECTION CIRCUIT
PRML SIGNAL PROCESSING CIRCUIT
24'
SIGNAL DETERMINATION CIRCUIT
25
READ CLOCK
WRITE CLOCK
WOBBLE CLOCK
WRITE DRIVER
31
32
SERVO CONTROLLER
35
OPTICAL PICKUP SECTION
22
34
1
SPINDLE MOTOR
33

FIG. 26

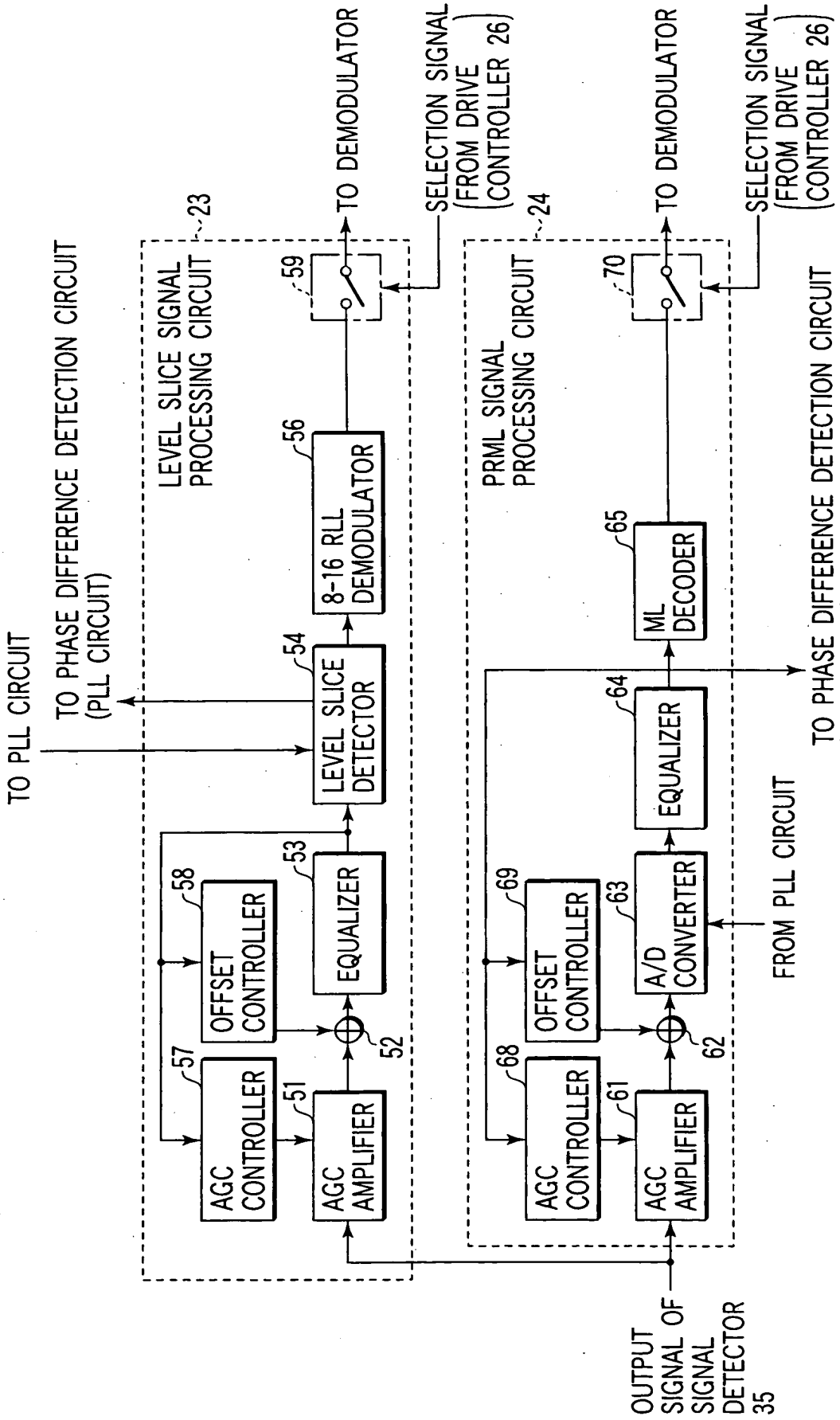

TO PLL CIRCUIT
TO PHASE DIFFERENCE DETECTION CIRCUIT (PLL CIRCUIT)
LEVEL SLICE SIGNAL PROCESSING CIRCUIT
23
AGC CONTROLLER
57
AGC AMPLIFIER
51
OFFSET CONTROLLER
58
EQUALIZER
53
52
LEVEL SLICE DETECTOR
54
8-16 RLL DEMODULATOR
56
59
TO DEMODULATOR
SELECTION SIGNAL (FROM DRIVE CONTROLLER 26)
PRML SIGNAL PROCESSING CIRCUIT
24
AGC CONTROLLER
68
AGC AMPLIFIER
61
OFFSET CONTROLLER
69
A/D CONVERTER
63
62
EQUALIZER
64
ML DECODER
65
70
TO DEMODULATOR
SELECTION SIGNAL (FROM DRIVE CONTROLLER 26)
FROM PLL CIRCUIT
TO PHASE DIFFERENCE DETECTION CIRCUIT (PLL CIRCUIT)
OUTPUT SIGNAL OF SIGNAL DETECTOR 35

FIG. 27

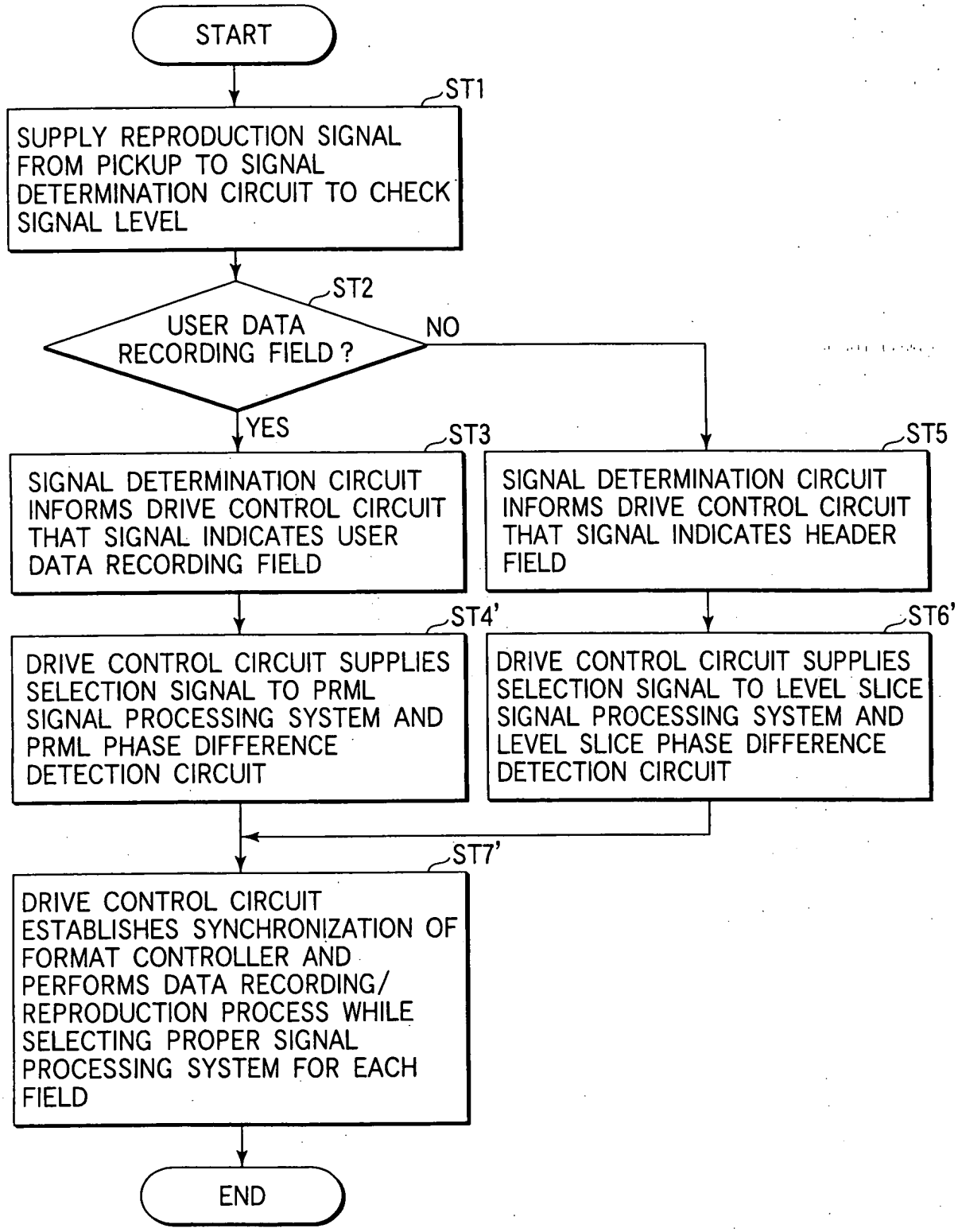

START
ST1
SUPPLY REPRODUCTION SIGNAL FROM PICKUP TO SIGNAL DETERMINATION CIRCUIT TO CHECK SIGNAL LEVEL
ST2
USER DATA RECORDING FIELD ?
NO
YES
ST3
SIGNAL DETERMINATION CIRCUIT INFORMS DRIVE CONTROL CIRCUIT THAT SIGNAL INDICATES USER DATA RECORDING FIELD
ST5
SIGNAL DETERMINATION CIRCUIT INFORMS DRIVE CONTROL CIRCUIT THAT SIGNAL INDICATES HEADER FIELD
ST4'
DRIVE CONTROL CIRCUIT SUPPLIES SELECTION SIGNAL TO PRML SIGNAL PROCESSING SYSTEM AND PRML PHASE DIFFERENCE DETECTION CIRCUIT
ST6'
DRIVE CONTROL CIRCUIT SUPPLIES SELECTION SIGNAL TO LEVEL SLICE SIGNAL PROCESSING SYSTEM AND LEVEL SLICE PHASE DIFFERENCE DETECTION CIRCUIT
ST7'
DRIVE CONTROL CIRCUIT ESTABLISHES SYNCHRONIZATION OF FORMAT CONTROLLER AND PERFORMS DATA RECORDING/ REPRODUCTION PROCESS WHILE SELECTING PROPER SIGNAL PROCESSING SYSTEM FOR EACH FIELD
END

FIG. 28

HEADER FIELD					
VFO1	AM	PID1	IED1	PA1	AM
36	3	4	2	1	3

71

FIG. 29

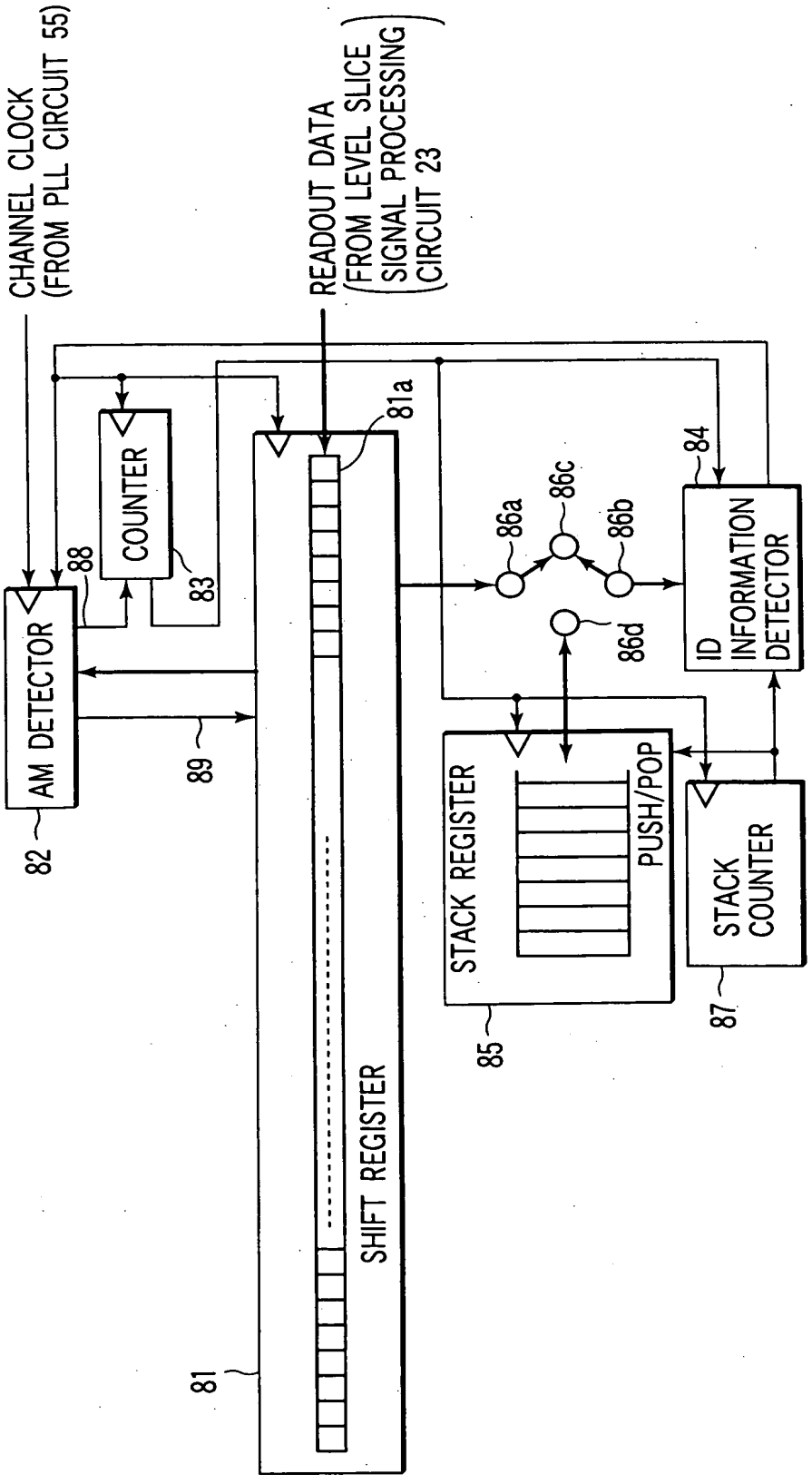

CHANNEL CLOCK
(FROM PLL CIRCUIT 55)
READOUT DATA
(FROM LEVEL SLICE
SIGNAL PROCESSING
CIRCUIT 23
81a
COUNTER
83
88
AM DETECTOR
82
89
86a
86c
86b
86d
84
ID
INFORMATION
DETECTOR
STACK REGISTER
PUSH/POP
85
STACK
COUNTER
87
SHIFT REGISTER
81

FIG. 30

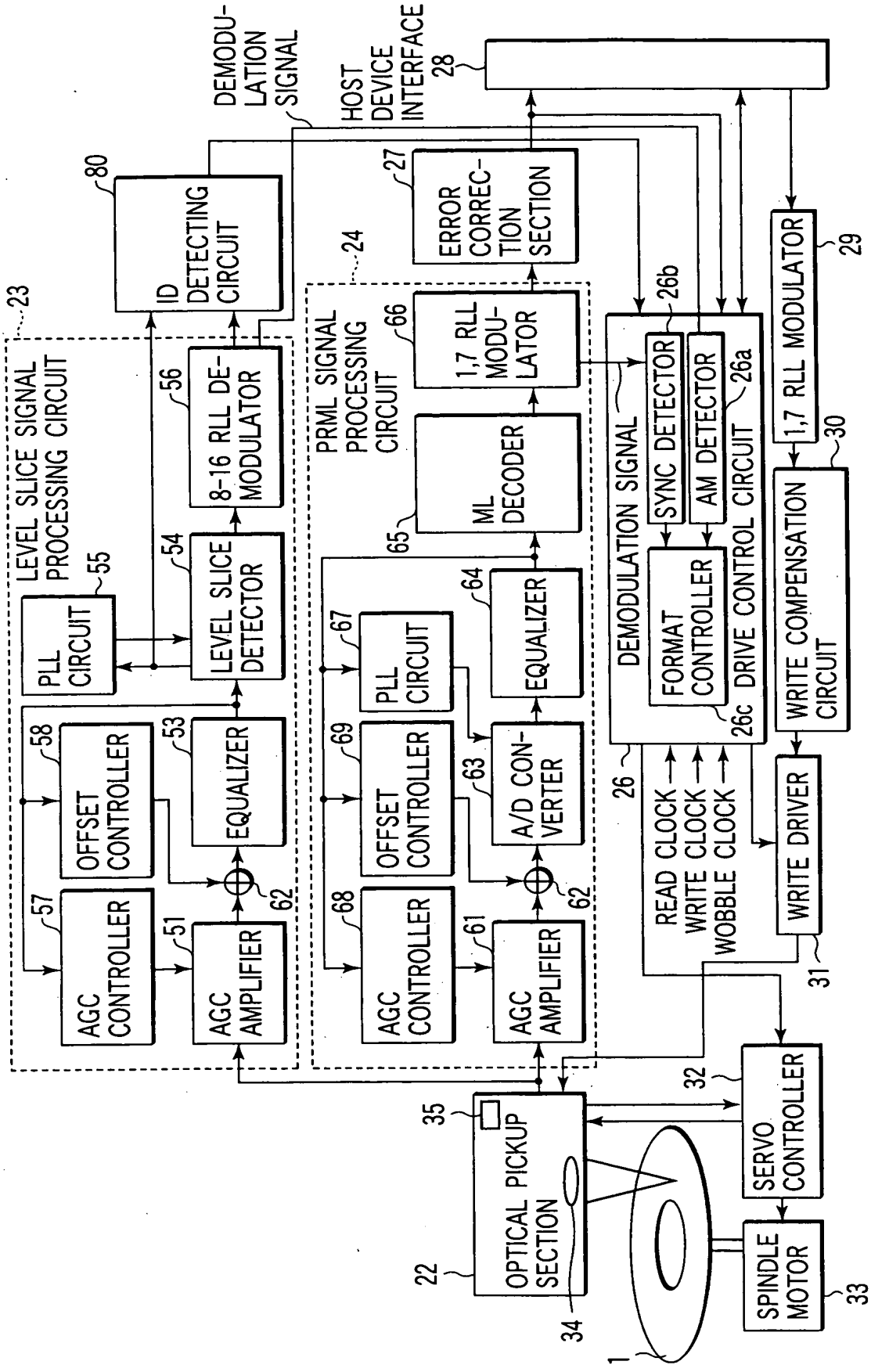

DEMODU-
LATION
SIGNAL
HOST
DEVICE
INTERFACE
28
80
ID
DETECTING
CIRCUIT
27
ERROR
CORREC-
TION
SECTION
23
24
LEVEL SLICE SIGNAL
PROCESSING CIRCUIT
PRML SIGNAL
PROCESSING
CIRCUIT
66
1,7 RLL
MODU-
LATOR
26b
29
56
8-16 RLL DE-
MODULATOR
65
ML
DECODER
SYNC DETECTOR
AM DETECTOR
26a
1,7 RLL MODULATOR
30
55
PLL
CIRCUIT
54
LEVEL SLICE
DETECTOR
67
PLL
CIRCUIT
64
EQUALIZER
DEMODULATION SIGNAL
FORMAT
CONTROLLER
26c DRIVE CONTROL CIRCUIT
WRITE COMPENSATION
CIRCUIT
58
OFFSET
CONTROLLER
53
EQUALIZER
69
OFFSET
CONTROLLER
63
A/D CON-
VERTER
57
AGC
CONTROLLER
51
AGC
AMPLIFIER
62
68
AGC
CONTROLLER
61
AGC
AMPLIFIER
62
26
READ CLOCK
WRITE CLOCK
WOBBLE CLOCK
WRITE DRIVER
31
35
32
OPTICAL PICKUP
SECTION
SERVO
CONTROLLER
22
34
1
SPINDLE
MOTOR
33

FIG. 31

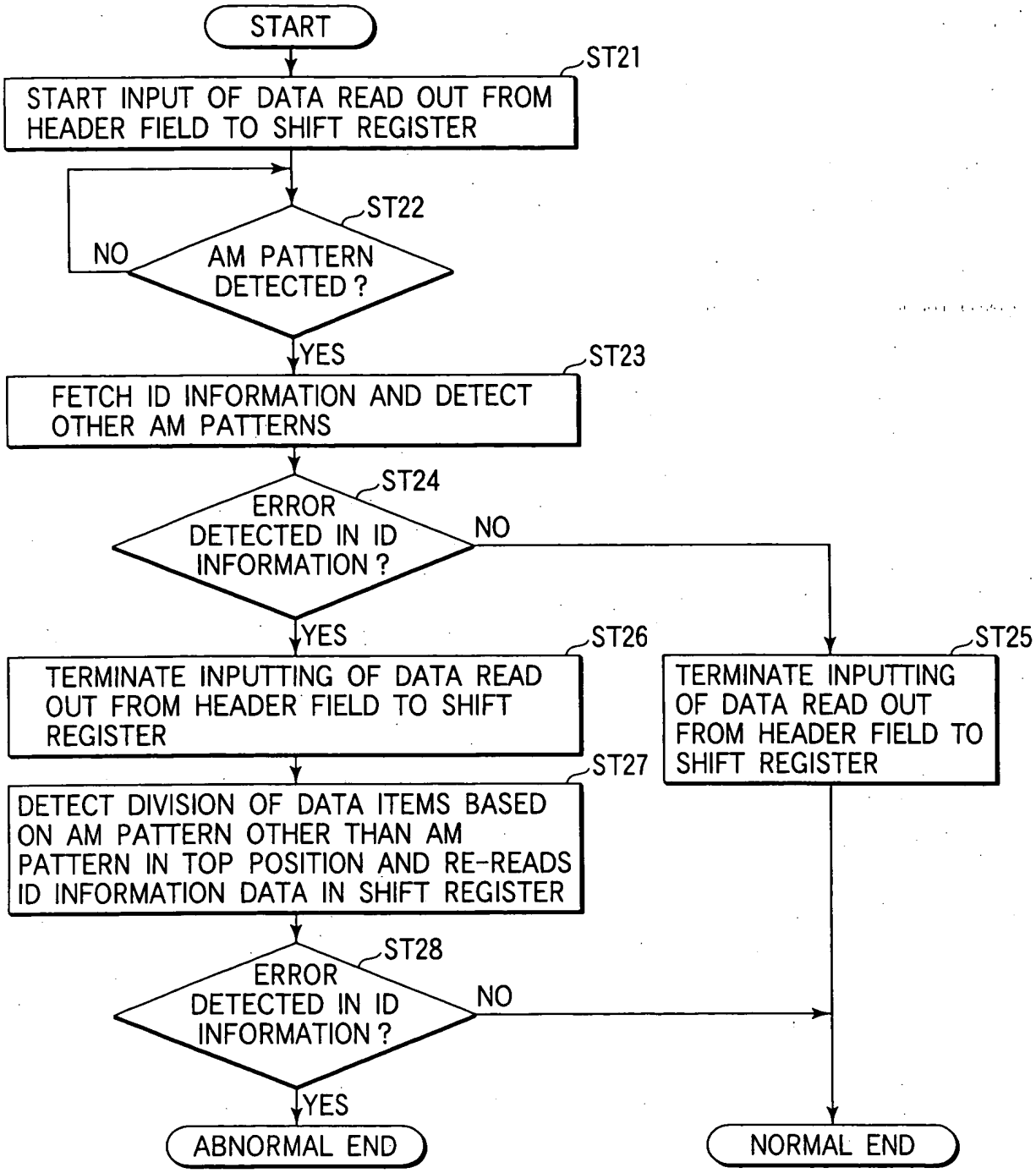

START
ST21
START INPUT OF DATA READ OUT FROM HEADER FIELD TO SHIFT REGISTER
ST22
NO
AM PATTERN DETECTED ?
YES
ST23
FETCH ID INFORMATION AND DETECT OTHER AM PATTERNS
ST24
ERROR DETECTED IN ID INFORMATION ?
NO
YES
ST26
TERMINATE INPUTTING OF DATA READ OUT FROM HEADER FIELD TO SHIFT REGISTER
ST25
TERMINATE INPUTTING OF DATA READ OUT FROM HEADER FIELD TO SHIFT REGISTER
ST27
DETECT DIVISION OF DATA ITEMS BASED ON AM PATTERN OTHER THAN AM PATTERN IN TOP POSITION AND RE-READS ID INFORMATION DATA IN SHIFT REGISTER
ST28
ERROR DETECTED IN ID INFORMATION ?
NO
YES
ABNORMAL END
NORMAL END

FIG. 32

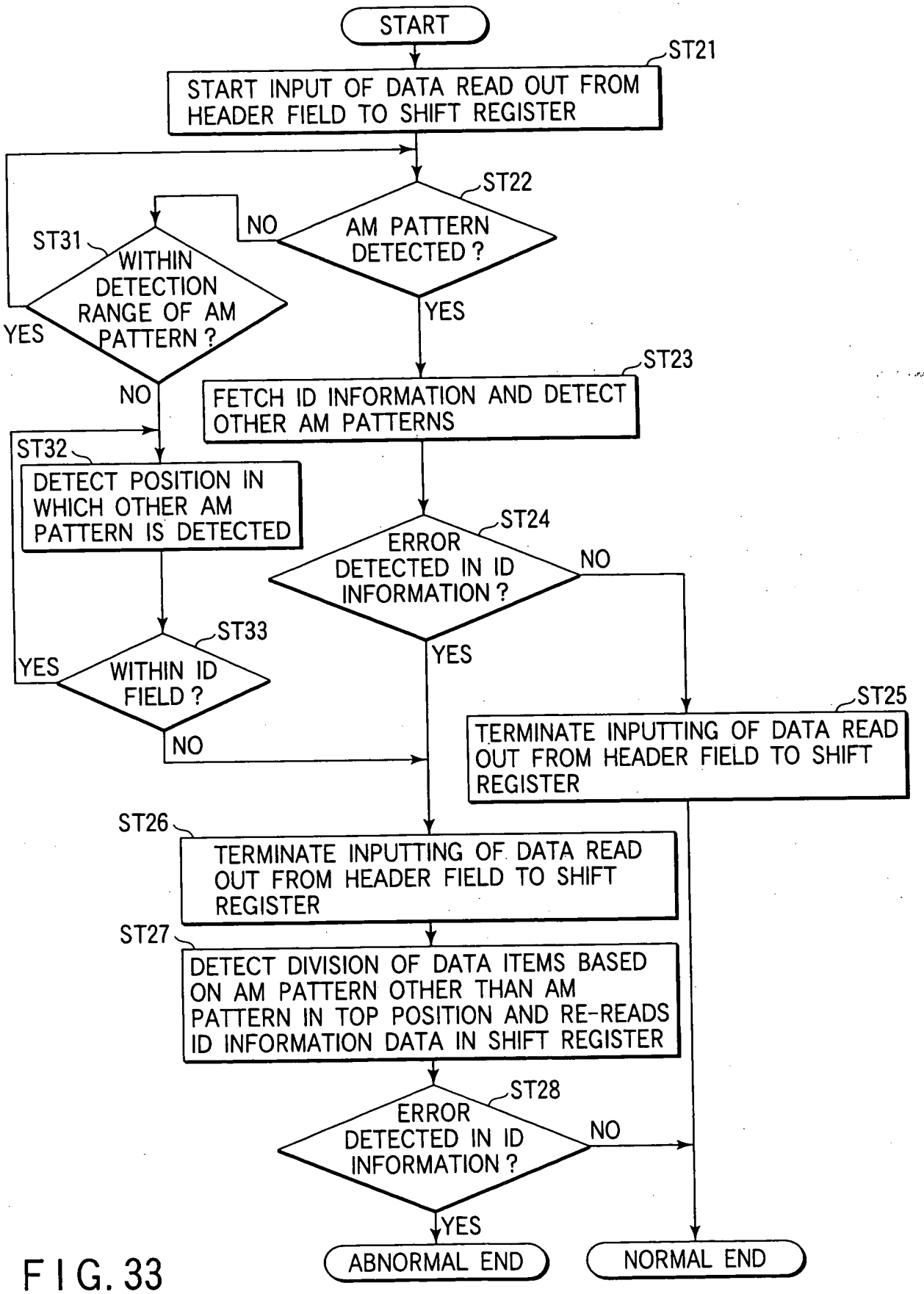

START
ST21
START INPUT OF DATA READ OUT FROM HEADER FIELD TO SHIFT REGISTER
ST22
AM PATTERN DETECTED ?
NO
YES
ST31
WITHIN DETECTION RANGE OF AM PATTERN ?
YES
NO
ST23
FETCH ID INFORMATION AND DETECT OTHER AM PATTERNS
ST32
DETECT POSITION IN WHICH OTHER AM PATTERN IS DETECTED
ST24
ERROR DETECTED IN ID INFORMATION ?
NO
YES
ST33
WITHIN ID FIELD ?
YES
NO
ST25
TERMINATE INPUTTING OF DATA READ OUT FROM HEADER FIELD TO SHIFT REGISTER
ST26
TERMINATE INPUTTING OF DATA READ OUT FROM HEADER FIELD TO SHIFT REGISTER
ST27
DETECT DIVISION OF DATA ITEMS BASED ON AM PATTERN OTHER THAN AM PATTERN IN TOP POSITION AND RE-READS ID INFORMATION DATA IN SHIFT REGISTER
ST28
ERROR DETECTED IN ID INFORMATION ?
NO
YES
ABNORMAL END
NORMAL END

FIG. 33

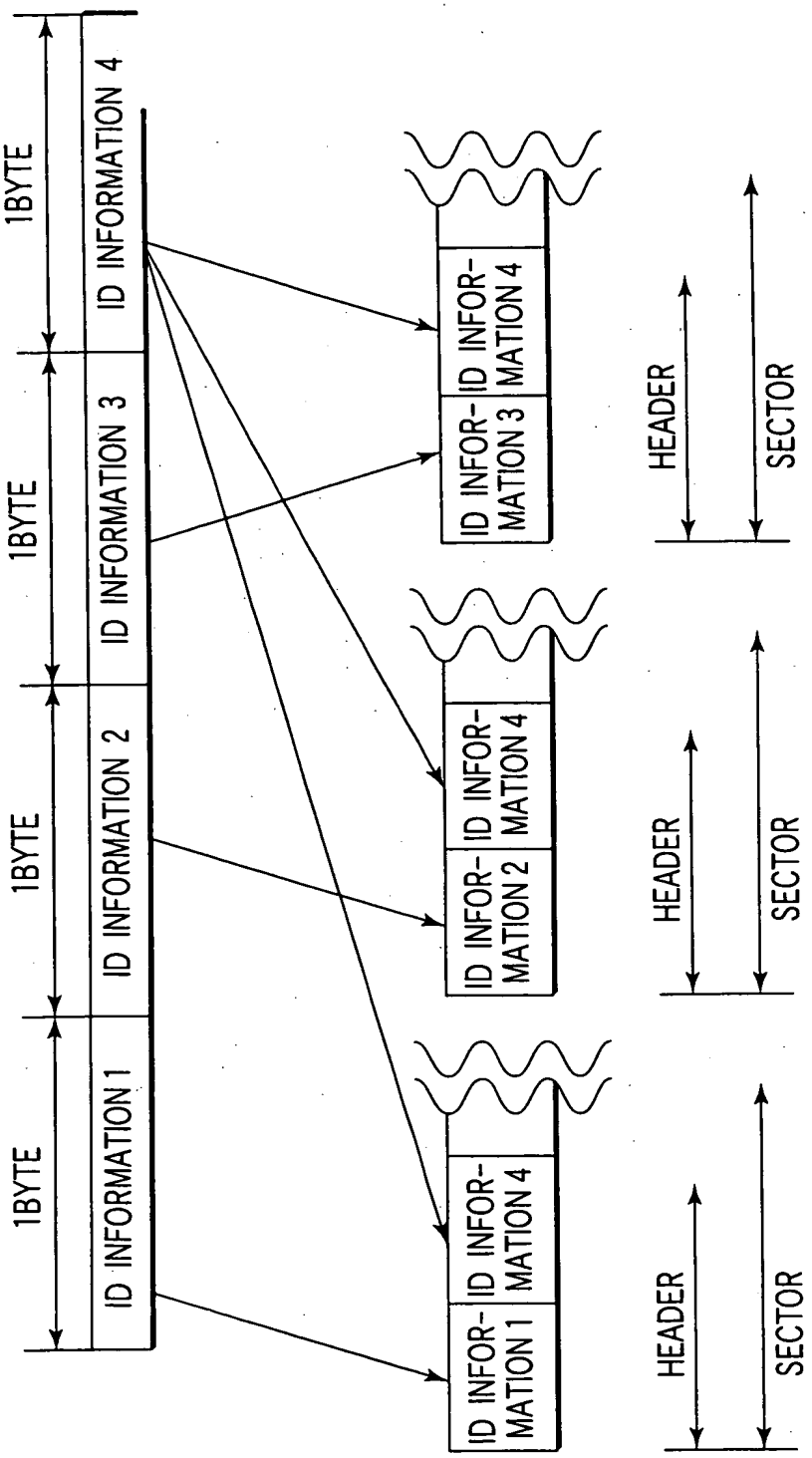

1BYTE
ID INFORMATION 4
1BYTE
ID INFORMATION 3
1BYTE
ID INFORMATION 2
1BYTE
ID INFORMATION 1
ID INFOR-MATION 4
ID INFOR-MATION 3
ID INFOR-MATION 4
ID INFOR-MATION 2
ID INFOR-MATION 4
ID INFOR-MATION 1
HEADER
SECTOR
HEADER
SECTOR
HEADER
SECTOR

FIG. 34

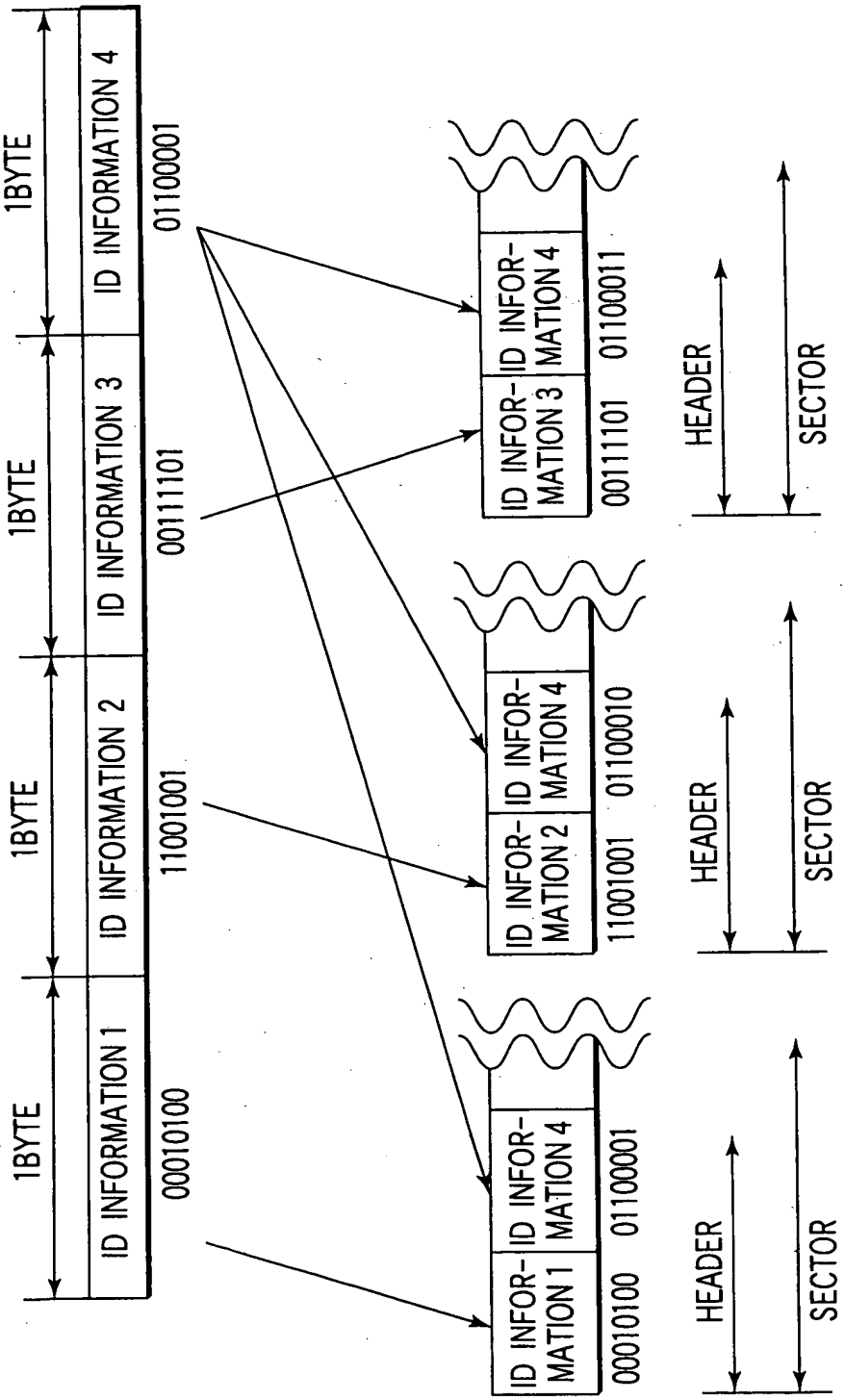

1BYTE
ID INFORMATION 1
ID INFORMATION 2
ID INFORMATION 3
ID INFORMATION 4
00010100
11001001
00111101
01100001
ID INFOR-MATION 1
ID INFOR-MATION 2
ID INFOR-MATION 3
ID INFOR-MATION 4
01100010
01100011
HEADER
SECTOR

FIG. 35